VALLURUPALLI NAGESWARA RAO VIGNANA JYOTHI
INSTITUTE OF ENGINEERING AND TECHNOLOGY
An Autonomous, ISO 9001:2015 & QS I-Gauge Diamond Rated Institute, Accredited by NAAC with 'A++' Grade
NBA Accreditation for B.Tech. CE, EEE, ME, ECE, CSE, EIE, IT Programmes
Approved by AICTE, New Delhi, Affiliated to JNTUH, NIRF 135th Rank in Engineering Category
Recognized as "College with Potential for Excellence" by UGC
Vignana Jyothi Nagar, Pragathi Nagar, Nizampet (S.O), Hyderabad – 500 090, TS, India.
Telephone No: 040-2304 2758/59/60, Fax: 040-23042761
E-mail: postbox@vnrvjiet.ac.in, Website: www.vnrvjiet.ac.in
Estd.1995

Department of ECE
Center for VLSI

About the Center

The center for VLSI is established in the year 2010 with an objective of inculcating the reaerch culture in the field of VLSI among students and faculty. This center has spread its activities to research areas like Analog and Mixed Signal Design, Radio Frequency Integrated Circuit (RFIC) Design, Low-Power VLSI Design and Algorithms, etc. The center has PG programme in VLSI System Design with an intake of 18. A group of 14 faculty with the specialization of VLSI and, are working in the areas of Low Power VLSI, Design verification and testing, physical design, FPGA implementations of high performance systems and VLSI signal processing. One full time Ph.D scholar admitted under National Doctoral Fellowship offered by AICTE, India is working in the area of low power VLSI. The VLSI center is equipped with licensed softwares like Synopsys frontend and backend bundle, Mentor Graphics tool and latest FPGA kits.

Faculty associated with Center for VLSI

S. No	Name of the faculty	Designation	Area of research
1	Dr. S. Rajendra Prasad	Professor, Head of ECE	Circuit Design using Emerging Technologies, Circuit Design Based Nanotechnology, Low Power VLSI
2	Mr. A. Ramesh Kumar	Associate Professor	VLSI Signal processing
3	Dr. P. Kishore	Associate Professor	Analog & Digital Low Power VLSI
4	Ms. J.L.V. Ramana Kumari	Assistant Professor	VLSI Verification & Testing
5	Ms. G. Shanthi	Assistant Professor	VLSI, MEMs
6	Mr. K. Sarath Chandra	Assistant Professor	Low Power VLSI
7	Dr. Priyanka Veeramosu	Assistant Professor	VLSI Signal Processing
8	Ms. L. Dharma Teja	Assistant Professor	Low Power VLSI

9	Mr. Ch. Ganesh	Assistant Professor	Low Power VLSI
10	Ms. K. Swetha Reddy	Assistant Professor	Semi-Custom IC Design, Low Power VLSI
11	Ms. S. Naga Leela	Assistant Professor	Low Power VLSI
12	Mrs. N.Neelima	Assistant Professor	VLSI Signal processing
13	Dr. A Sai Kumar	Assistant Professor	Low power VLSI
14	Mr. E. Vijaya Babu	Assistant Professor	VLSI Signal processing

Facilities

Center for VLSI has two laboratories with the following softwares and hardware kits. The facilities are available for all faculty and students who would like to participate in VLSI R&D activities.

Softwares

- Xilinx Vivado System Edition Software
- Mentor Graphics HEP1 Tool
- Synopsis Tool

Hardware Kits

- Atlys Spartan 6 FPGA Kit : 05
- Artix-7 Nexys 4 DDR Kit : 02
- Zynq Board(Zynq Zed Development Kit) : 01
- Zynq Video And Image Processig Kit : 01
- Zynq 7000epp Evaluation Kit : 01
- Spartan 605 Kit : 01
- Spartan 3E FPGA Kit : 01
- Anvyl Kit : 01

Funded research projects carried out in center for VLSI

S.No	Title of the Project	Funding Agency	Sanctioned Amount in Lakhs	Faculty Associated
1	Design an FFT/IFFT IPcore with run-time configurable FFT size and data type and compile time configurable data type and data precision.	MMRFIC Technologies Pvt. Ltd	2.0	Mr. Ch. Ganesh
2	Development of low power and high speed FPGA based IP core mini Ace architecture compatible to data device corporation	AICTE/RPS	14.35	Dr.P.Kishore
3	IP Core Development Of MIL STD 1553 for RT and MT Terminals”	Ananth Technologies Ltd	4.24	Dr.P.Kishore Mr.K.Sarath Chandra Mrs.K.Sweth a Reddy

Faculty as Resourse Persons

S. No.	Name of the program	Lecture Topic	Name of the Faculty	Duration	Venue	Organized by
1	Webinar	Strategies and tools to avoid plagiarism	Dr.Ranjan K Senapathi	23-06-2021	VVP Institute of Engineering and Technology	VVP Institute of Engineering and Technology
2	Guest Lecture	Introduction to Communication & Signal Processing	Dr.S.Rajendra Prasad	03-06-2021	Annamacharya Institute of Technology and Sciences, Kadapa, AP	Annamacharya Institute of Technology and Sciences, Kadapa, AP
3	VLSI Training Program	VLSI Evolution and Recent trends in VLSI industry	K.Sarath Chandra	17-05-2021 to 28-07-2021	Dept. of ECE, VNRVJIET	VNRVJIET
4	VLSI Training Program	FPGA Design Flow ASIC Design Flow Designing with FPGAs Hands on session with Verilog HDL IC Design Flow-Semicustom and Full custom design-Hands on Session Overview of Digital Design Introduction to Verilog HDL, Language Constructs and Conventions	K.Naresh	17-05-2021 to 28-07-2021	Dept. Of ECE, VNRVJIET	VNRVJIET
5	VLSI Training Program	Gate Level Modeling Designing with Pseudo NMOS, NMOS enhancement and Depletion mode transistors CMOS,Pass Transitor Logic, Complementary PTL, Transmission Gate Logic Data Flow Level Modeling	Dr.P.Kishore	17-05-2021 to 28-07-2021	Dept. Of ECE, VNRVJIET	VNRVJIET
6	VLSI Training Program	Behavioral Modeling Hands on Sessions on Digital Design 7with Verilog Functions, Tasks, and User-Defined Primitives	K.Swetha Reddy	17-05-2021 to 28-07-2021	Dept. Of ECE, VNRVJIET	VNRVJIET
7	VLSI Training	FF Conversions & Synchronous	J.L.V.Ramana Kumari	17-05-2021 to 28-07-	Dept. of ECE, VNRVJIET	VNRVJIET

	Program	Asynchronous counter Design Mealy and Moore type FSMs with examples Introduction to Design of Controller and Data path systems. Design of serial Receiver and Transmitter Sequence detector design.		2021		
8	VLSI Training Program	Hands on Sessions on Digital Design with Verilog	Ch. Ganesh	17-05-2021 to 28-07-2021	Dept. of ECE, VNRVJIET	VNRVJIET
9	VLSI Training Program	IC Design Flow-Semicustom and Full custom design-Hands on Session MOS FET Characteristics	Dr.S. Rajendra Prasad	17-05-2021 to 28-07-2021	Dept. of ECE, VNRVJIET	VNRVJIET
10	IoT training Program	CMOS inverter - static and dynamic characteristics	Aytha Ramesh Kumar	17-05-2021 to 28-07-2021	Dept. of ECE, VNRVJIET	VNRVJIET
11	5-Day Online National Workshop on “Recent Trends in Microelectronic Devices, VLSI Circuits and their applications-	Design of serial Receiver and Transmitter	Dr.S.Rajendra Prasad	25-01-2021 to 29-01-2021.	KL University	KL University
12	National Level Faculty Development Programme on “ Recent trends in Electronics and Communications for Teaching Learning and Research”	Recent trends in Electronics and Communications	Dr.S.Rajendra Prasad	28-12-2020 to 31-12-2020	Sridevi Women’s Engineering College	Sridevi Women’s Engineering College
13	Two day webinar on "Present Trends and Research scopes in SG Wireless Communications	Evolution of Wireless Technologies	Dr. S. Rajendra Prasad	27-06-2020	G.Pulla Reddy Engineering College, Kurnool.	G.Pulla Reddy Engineering College, Kurnool.
14	RTL design and	VLSI Evolution and Recent trends in	K. Sarath	09-06-2020	Dept. of ECE, VNRVJIET	VNRVJIET

	verification	VLSI industry	Chandra			
15		Classification of IC Design	K. Sarath Chandra	16-06-2020		
16	RTL design and verification	Controller design using FSMs	J LV Ramana kumari	12-06-2020	Dept. of ECE, VNRVJIET	VNRVJIET
17	RTL design and verification	VLSI Design flow(FPGA& ASIC)	K. Naresh	17-06-2020	Dept. of ECE, VNRVJIET	VNRVJIET
18		Behaviour modelling style of Verilog HDL (Hands-on)		19-06-2020		
19	RTL design and verification	Structural Modelling style of Verilog HDL (Hands-on)	Ch. Ganesh	22-06-2020	Dept. of ECE, VNRVJIET	VNRVJIET
20		FPGA implementation of Digital system(Case Study)		25-06-2020		
21	RTL design and verification	Importance of Verilog HDL in Digital Design Automation	K. Swetha Reddy	18-06-2020	Dept. Of ECE, VNRVJIET	VNRVJIET
		Synthesizable Verilog HDL for FSM(Hands-on)		23-06-2020		
		Design Verification using Testbench(Hands-on)		24-06-2020		
22	Embedded Systems, Smart Sensors for IOT Applications	Overview on wireless sensors	Dr.S. Rajendra Prasad	17-09-2018 to 20-09-2018	Department of ECE, VNRVJIET	VNR VJIET
23	Embedded Systems, Smart Sensors for IOT Applications	FPGA & SoC Based Embedded Systems Designs	A.Ramesh Kumar	17-09-2018 to 20-09-2018	Department of ECE, VNRVJIET	VNR VJIET

Faculty as Reviewers and Editorial board members

S. No.	Name of the faculty	Nature of Contribution	Details of associated Organization / Journal / Conference etc.
1.	Dr.S.Rajendra Prasad	Editorial Board member	International Journal of VLSI Design & Communication System (VLSICS).
		Reviewer	Heliyon – a peer-reviewed open access journal - indexed by Scopus.
		Guest Editor	International Journal of Sensors and Sensor Networks (IJSSN) - Journal
		Reviewer	International journal of Circuit Theory and Applications
			IEEE - Transactions on Devices and Materials Reliability
			Elsevier - Microelectronics Journal
			Springer - Journal of Computational Electronics
			Springer Journal – Soft Computing
			International Journal of Speech Technology (IJST)
			International Journal of VLSI Design & Communication Systems
		Board of Studies Member	Kesav memorial Institute of Technology, Hyderabad
2.	Dr.P.Kishore	Member	CAS/EDS joint chapter, IEEE Hyderabad Section
		Member, Technical Program Committee	International Conference on Artificial Intelligence: Theory and Applications [AITA 2021]
		Reviewer	IEEE International Symposium on Circuits and Systems (ISCAS), Organizing by IEEE Circuits and Systems Society at Japan.
3.	K.Naresh	Reviewer	IEEE Transactions on VLSI Systems

Faculty Awards and Recognitions

S.No.	Name of the Faculty	Designation	Details of the award and recognition
1	Dr.S.Rajendra Prasad	Professor	Recognized as IEEE Senior Member
			One of the Toppers (In TOP 1%) in NPTEL exam on Microelectronics: Devices to Circuits conducted during July-October 2021.
2	Dr.P.Kishore	Associate Professor	Topper in NPTEL Exam –VLSI Signal Processing (January-April 2020) Exam conducted in October 2020.
			Recognized as IEEE Senior Member in April 2020.
			Received Dr. Sarvepalli Radha Krishna Distinguished Scientist Award-2021in appreciation of the dedication and commitment in Technology and Research in ECE conferred on 5th September 2021 by Center for Professional Advancement Continuous Education(CPACE)
3	Dr.V.Priyanka	Assistant Professor	Recognized as IEEE Senior Member in Apr 2020.
			Received an Exemplary Student Branch Award from IEEE Hyderabad section Student Activity Committee on 4th December 2021

Faculty Guiding PhD scholars

S. No	Name of the faculty	Specialization	Ph.D. Details - (University & Year of Award)	Research Scholar Details			Status
				Name of the Research Scholar	Year of Admission and / or Completion	University	
1	Dr.S. Rajendra Prasad	Low Power VLSI	JNTUH,2015	S.Sravanthi	2017	JJTU, Rajasthan	On going
				Uma Maheswar	2019	AICTE-NDF	On going
				L.Dharma Teja	2011	JNTUH	On going
				Prasanna Kumar G	2017	SSSUT&MS, Sehore, MP	On going

Details of Faculty Professional Body Memberships

S. No	Faculty Name	Membership No.						
		IEEE	ISTE	IETE	ISOI	IEI	Internet Society	OTHERS
1	Dr.S.Rajendra Prasad	SM92175569	LM 107789	M202253	-	-	-	-
2	A.Ramesh Kumar	-	LM62868	M159839	-	-	-	
3	J.L.V.Ramana Kumari	97531144	LM62871	M234464	-	-	-	-
4	Dr.L.V.Rajani Kumari	97511211	LM79575	M234471	-	-	2236865	IAENG:293359
5	L.Dharma Teja	-	LM79578	M234473	-	-	-	-
6	G.Shanthi	-	LM 107791	-	-	-	2236857	IAENG: 293351
7	Dr. V. Priyanka	SM95145416	LM90973	AM234512	-	-	2229846	IAENG:293357
8	Dr. P. Kishore	SM95145372	LM71521	AM198519	-	AM1001704	-	-
9	K.Sharath Chandra	-	LM 107792	-	-	-	2236868	IAENG:293371
10	Ch.Ganesh		LM 122048	-	-	-	-	
	K.Swetha Reddy	97531079	LM 122058	-	-	-	2236863	IAENG:293333
	S.Naga Leela	-	LM 107784	-	-	-	-	IAENG:293363

Industry interactions

List of MOUs with VLSI industries

Sl. No.	Name of the industry	Impact
1	Ananth Technologies Ltd.	Sanctioned consultancy project on "IP Core Development of MIL STD 1553 for RT and MT terminals" for an amount of Rs.4.24 Lakhs.
2	AMD Ltd	P.G (VLSI System Design) students got internship opportunities in VLSI domine during academic year
3	AVANTEL Ltd	Dr. A. Vidyasagar, Managing Director is a member of BoS and involving in design the syllabus of courses under communication module.
4	TCS, Hyderabad	➢ Remote Internships are provided to the students. ➢ P.G (VLSI System Design) students got internship opportunities in VLSI domine during academic year 2021-22, , which is a new initiative of TCS Hyderabad.

List of Industry personels associated

1. Mr. Venu Gopal Bhat, Director of Engineering, Automotive SW, NVIDIA,Bangalore
2. Mr. Lakshmi Narayana kamarthi, Principal Engineer, NXP India Private Limited,Bangalore
3. Mr. K.Balaji, Director of Physical Design, SiFive Ltd,Bangalore
4. Mrs.Vijitha Challa, Pre-Si valid/verif engineer, INTEL, Hyderabad
5. Mr.D. Sreekanth, Application Engineer,AMD India Private Limited, Hyderabad
6. Mr.Tummuri Bala Surya Sriramachandra Pavan Kumar, Soc Design Engineer, INTEL
7. Mr.S.Krishna Teja, Staff Engineer, Mentor Graphics, Hyderabad
8. Mr.Yadagiri D, Sr. Silicon Design Engineer ,AMD India Private Limited, Hyderabad
9. Mr.Bala Krishna ,Synopsys,Hyderabad
10. Mr. Sai Teja Mannam,SoC Design Engineer,Intel, Hillsboro, Oregon, USA
11. Dr.E.Lakshmi Prasad,Senior DFT Engineer, Tessolve semiconductor Pvt. Ltd, Bangalore
12. Mr. Suresh Nagula, SR II, R&D Engineer,Synopsys Inc, Hyderabad
13. Dr.Srinivas, Design Engineer, Micron Technology Inc, Hyderabad
14. Nagalatha Ramineni, Systems Design Manager, AMD India Private Limited, Hyderabad
15. Dr.A.G.Krishnaknath, Senior Manager,AMS Semiconductors Pvt Ltd, Hyderabad.

Guest lectures delivered by Industry experts during last 3 Years

S.No	Name of the industry personal	Industry associated	Title	Date
1	Mr. s. Krishna Teja	Siemens EDA, Hyderabad	Design Challenges in Digital VLSI	25th June 2022
2	Mr. D.Yadagiri	Advanced Micro Devices(AMD)Ltd, Hyderabad	Bridging gap between Industry and Academia	29-08-2020
3	Mr.Y.Avinash	Mirafra Technologies Ltd, Bangalore	Engineering Education - Match Your Passion - Charting the Right Career Choice	19-09-2020
4	Mr.D. Srikanth	Xilinx, Hyderabad	Carrier Opportunities	19-12-2020
5	Ms. Sushmitha Ch	Synopsys, Hyderabad	Experience & Tips During Placements, Balancing and Learning During Post Placement	02-06-2021
6	Mr.Yadagiri	Advanced Micro Devices(AMD)Ltd, Hyderabad	Motivating the students towards the Carrier in VLSI Industry	23-11-2019

Guest Lecture delivered on " Opportunities and Challenges in VLSI Industry" by Mr.Lakshmi Narayana Kamarthi

Guest Lecture delivered on "Carrier Opportunities" by Mr.D. Srikanath

Internships Opportunities in VLSI related industries

S.No	Name of the Industry	Name of the Student & Roll No
1	Synopsys	Sahithi Kannaiahgari(17071A0421)
2		Shivani Samanapally(17071A0447)
3		Rohith Reddy Appidi(17071A0463)
4		Saadia Hassan(17071A0446)
5		Sai Sharan Morisetty(19075A0406)
6		Rupa Sreelekha M(18071A0493)
7		Samarth Raj G(18071A04B4)
8		Challapalli Ramakrishna(18071A04D3)
9	Advanced Micro Devices(AMD)	Kota Murali Mohan(20071D5703)
10		Y Sravya Mounika(20071D5711)
11		Adapa Naga Sai Nikhil(18071D5701)
12	TCS	Sai Teja Tuduru(20071D5708)
13		M. Sai Greeshma(19071D5708)
14	Siliconus Technologies Pvt Ltd	Sainath Yarra(20071D5709)
15		Nagasani Rakesh(20071D5706)
16		Harsha Lourdu M(20071D5705)
17		Kacharla Sanjay(20071D5702)
18	Mentor Graphics	P.Sravanthi(19071D5711)

**All the students are converted to full time employees

Academic projects carried out by Student Projects during 2021-22

Batch No.	Roll No.	Title of the Project	Name of the Supervisor
1	18071A0402	Multicock domain based watch dog timer for image processor	Ms.J.L.V.Ramana Kumari
	18071A0455		
	18071A0411		
	19075A0402		
	17071A0458		
2	18071A0401	Design and Analysis of CMOS two stage comparator	Dr.S.Rajendra Prasad
	18071A0413		
	18071A0421		
	18071A0424		
3	18071A0443	15T SRAM cell using CNTFET,FINFET & GNRFET	Ms.L.Dharma Teja
	418071A0403		
	18071A0418		
	18071A0405		
4	18071A0492	Design and Analysis of Logic Circuits Using Quantum Dot Cellular Automata	Ms.K.Swetha Reddy
	18071A04A6		
	18071A04B6		
	18071A04B8		
5	18071A0478	Area Effiecient Adder using QCA	Dr.P.Kishore
	18071A0486		
	18071A0491		
	18071A04A0		
6	18071A0462	Design and Analysis of Modified Strong-Arm Latch comparator	Ms.K.Swetha Reddy
	18071A0482		
	18071A0493		
	18071A0494		
	18071A04A9		
7	18071A04A5	Impelemnatation of cascaded integrator comb filter using verilog hdl	Ms.G.Shanthi
	18071A04B4		
	19075A0409		
	19075A0410		
8	18071A0461	Design of AHBtoAPB Bridge for efficient power consumption	Mr.K.Sarath Chandra
	18071A0487		
	18071A0490		
	18071A04A1		
9	18071A0497	Low power and low area VD-FIR filter	Dr.V.Priyanka
	18071A0476		
	18071A0463		
	18071A04C0		
	16071A04A5		
10	18071A04F1	Design of Domino Comparator using CNTFET	Ms.S.Naga Leela
	18071A04C8		
	19075A0415		
	18071A04E5		
11	18071A04D1	Dynamic Reconfigurable FIR filter for 5G Applications	Mr.A.Ramesh Kumar
	18071A04F3		
	18071A0H8		
	19075A0417		
12	18071A04E6	Design of Approximate divider arithemtic circuit for image processing applications	Mr.Ch.Ganesh
	18071A04D8		

	18071A04D7		
	18071A04H1		
13	18071A04G3	Design and analysis of cmos voltage controlled LC Oscillator	Dr.S.Rajendra Prasad
	18071A04C6		
	18071A04F9		
	18071A04D3		
14	18071A04C9	Implementation of error detection and correction using viterbi decoding	Mr.Ch.Ganesh
	18071A04G1		
	18071A04H6		
	18071A04J0		
15	18071A04K1	Design of FIR filter based on retiming using vlsi design metrics	Dr.P.Kishore
	18071A04M7		
	18071A04N0		
	18071A04M9		
16	18071A04N5	Design of 4-bit Approximate Dadda Multiplier for CNN Applications	Mr.K.Nareh
	18071A04K7		
	19075A0419		
	18071A04M0		

Best academic projects from the Center for VLSI for the academic year 2020-21

S.No.	Project Title	Roll Nos	Description
1	Design and Analysis of Logic Circuits Using Quantum Dot Cellular Automata	18071A0480 18071A0467 18071A04B3 18071A0469	Quantum-dot Cellular Automata (QCA) is a substitution to Complementary Metal–Oxide– Semiconductor (CMOS) technology in nanoscale level. With technology scaling, high power consumption of design prevents the energy-efficient realization of complex logic circuits at nanoscale. This system works on the basis of electron interactions within quantum dots rather than columbic force. This paper mainly projects the design and analysis of results of various logic circuits using quantum dot cellular automata (QCA) designer.
2	Design of FIR filter based on retiming using vlsi design metrics	18071A0492 18071A04A6 18071A04B6 18071A04B8	Retiming is a VLSI design technique in which the positioning or the arrangement of the delay elements or registers is reorganized such that the critical path delay of the filter is reduced. The rearrangement and addition of registers is such that the functionality of the retimed FIR filter is same as that of the original filter. Simulation results are discussed in this project. Optimized FIR filters are hence designed using different retiming techniques by maintaining a tradeoff between the design metrics in comparison with the existing designs.

Outcome of the Student Academic projects(2021-2022)

Papers published/communicated

S.No	Title of the Paper	Name of the Conference/Journal	Conference Dates	Status of the paper(Submiited/Accepted/Published)
1.	Convolution Merging Technique For Image Encryption Application	International Conference on Recent Trends in Microelectronics, Automation, Computing and Communication Systems(ICMACC-2022)	28-30 Decemebr 2022	Accepted
2.	Analyzing Performance Metrics of Low Power 15T Sram Cell Using Finfet And GNRFET	IJARIIE-ISSN(O)-2395-4396	2022	Published
3.	Area Efficient Logic Circuits using Quantun Dot Comuputation Automata	MIND 2022	21–22 December 2022	Submitted
4.	Implemenation of area Effiecient Adder using QCA	International Conference on Recent Trends in Microelectronics, Automation, Computing and Communication Systems	28–30 December 2022	Accepted
5.	An Efficient FPGA Implementation of Cascade Integrator Comb Filter	ICIIET 2022	22 - 24 September 2022	Submitted
6.	Design of Ahb2apb Bridge For Efficient Power Consumption	International Conference on Recent Trends in Microelectronics, Automation, Computing and Communication Systems	28–30 December 2022	Submitted
7.	An Efficient Approach for Denoising ECG Signal using FIR Filter	2022 International Conference on Intelligent Innovations in Engineering and Technology (ICIIET)	22-24 September 2022	Accepted
8.	Design and Analysis of CNTFET Dynamic Comparator	ICIECE-2022	DEC 16-17,2022	Submitted
9.	Implementation of Viterbi Decoder for Error Detection and Correction	IJRTI-Volume 7, Issue 8	August-2022	Published
10.	Design of FIR filter based on retiming using vlsi design metrics	ARPN Journal of Engineering and Applied Sciences (JEAS)	-	Submitted - Estimated time of publication- January 2023