Name: **KATTEKOLA NARESH**
Designation:Assistant Professor
Department:Electronics& Communication Engineering

Mail.I.D: naresh_k@vnrvjiet.in
Experience (in years): Teaching: 11 yrs Research: 00 Others (Industry): 00

1. Educational / Technical qualifications:

S.No	Level (UG / PG / Ph.D)	Year of passing	Specialization
1	Ph.D	pursuing	VLSI System Design
2	M. Tech	2010	VLSI System Design
3	B.Tech.	2007	ECE
4	Intermediate	2002	MPC
5	SSC	2000	NA

2. Teaching and Learning:

2.1. Teaching Interests:
Switching Theory and Logic Design, Linear and Digital IC, VLSI Design, Digital design Through Verilog, Low Power VLSI design, Electronic Measurements and Instrumentation, CPLD & FPGA Architectures & Applications

2.2.Novel Teaching and Learning Techniques adopted: POGIL,WIT & WIL and Learning by Doing.

2.3 Involvement in curriculum updating / Design:- B.Tech R18

3. Co-curricular and Extra-Curricular Activities

3.1. Interests and Hobbies:
Listening Music, Watching Cricket

3.2. CCA/ECA Organized: Poster presentation at Research and consultancy center in Convergence

3.3. CCA/ECA participated: Tech fests like project expo

- Texas Instruments project Competitions
- Freescale project Competitions
- 15 students from 4th year and 10 students from 1st Year

3.4. Counseling and Mentoring Activity:

- NBA work -Student Achievements and Participations.
- Member of Boards of Studies since 2018-19 academic year
- Mentoring students to choose emerging domains and aware them opportunities in their interested field (in project duration)
- Counseled many students for pursue higher studies to overcome their learning inhabitations.

3.5. Committees involved in:
Department level: Disciplinary committee member, PAAC Commitee, IQAC Coordinator
Institute Level:

4. Conference / Workshop / Seminar / Guest Lectures:

4.1. Conducted:

- The webinar series on RTL Design and Verification conducted by IEEE VNR CAS & SP Student Branch Chapters from June 9, 2020 to June 25, 2020.

- Two-week Online Faculty Development Programme on “Embedded UVM open-source Emulation & Functional Verification” from 13-24 July 2020.
- FDP-NKN Summer Course-2019 on “DEEP LEARNING AND APPLICATIONS” from 09th -13th December 2019.
- Training program on “Low Power VLSI Design using CAD Tools” from 28th October to 02nd November 2019.
- Summer FDP on “VLSI Chip Design Hands on using Open Source EDA” from 8th -12th July 2019.
- A Two Day workshop on “FPGA Design Flow using VIVADO”.
- A Three Day IACC 7th IEEE International Advance Computing Conference – Registration Committee.

4.2. Attended:

- Two weeks Online Faculty Development Programme on “Emerging Trends and Challenges in VLSI Mixed-Signal Processing for Fourth Industrial Revolution” from 08.02.2021 to 20.02.2021.
- Online 3-day FDP on "MIXED SIGNAL VLSI CIRCUIT DESIGN" Organized by Dept of ECE, Anurag Group of Institutions/ Anurag University, Hyderabad from 25 th to 27 th January 2021.
- Webinar on " VLSI Physical Design Using Mentor Graphics EDA Tools" Organized by CoreEL Technologies, Bangalore on 28 th January 2021.
- TWO WEEK AICTE Sponsored ONLINE FACULTY DEVELOPMENT PROGRAM on "Recent Trends in VLSI Design, Signal Processing & Optimization based on EDA tools" from 07-12-2021 to 19-12-2021.
- Xilinx Webinar on “Next Generation VLSI Design using Lower Technology Nodes” held on 4th Dec 2020.
- Online National Webinar on “Security Issues in IC Design Flow” on 18th Nov 2020.
- A Webinar on “Applications of Image Processing in Emerging Fields with Hands on Tutorial” on 14.08.2020.
- A Webinar on “Verilog HDL in Chip Design Cycle & Importance of Hardware Emulation” on 08.08.2020.
- Five Day online Professional Development Programme on “NBA IN A NUTSHELL” held from 27th to 31st Juy 2020.
- A webinar on “Automotive Embedded Systems” on 25.07.2020.
- Fiveday Online Faculty Development program on “Recent Trends in Nano Electronic Devices” from 13th to 17th July 2020.
- One-day Webinar on “Full Custom VLSI circuit design using Electric EDA Tool on 15th July 2020.
- A week workshop on “VNR Initiatives and Awareness on OBE” from 6th to 10th July 2020.
- Participated & completed successfully in a National Level Online FDP on "Image Processing and Computer Vision-Industrial Scope" from 8th to 12th July 2020.

- Participated in Xilinx Webinar on Custom IP Design and Validation Using Vivado held on 22nd May 2020 in association with CoreEL Technologies and Xilinx.
- One-day international webinar on "Navigation Satellite for modern telecommunications" on 11.07.2020.
- Participated and successfully completed Online Quiz on "Electronic Core Engineering Upskilling Test Series - Part 2" conducted during 6th - 10th June 2020.
- A week FDP on "LaTeX & Technical Report Writing" from 25th to 30th May 2020.
- A Five Day FDP on "Establishing Research Beyond Horizon" from 26th to 30th May 2020.
- Webinar on "Relax, Refresh, Rejuvenate" on 30th April 2020.
- Webinar on "Latex – A Scientific Documenting Tool" on 21st May 2020.
- "Xilinx Webinar on Custom IP Design and Validation Using Vivado" on 22nd May 2020.
- Webinar on "TACKLING ANXIETY IN THE CONTEXT OF IMPULSIVE ADAPTATION TO VIRTUAL CLASSROOM" on 20th May 2020.
- FDP-NKN Summer Course-2019 on "Python programming with Industry Perspective" from 2nd to 6th December 2019.
- A three Day FDP on "Designing with ZYNQ SOC and it's applications" from 16th to 18th October 2019.
- A One Week FDP on "Sensor Networks and IoT" from 26th to 31stAugust 2019.
- Summer FDP on "Introduction to Programming: A Pedagogical Approach" from 17th June 2019 to 21st June 2019.
- Summer FDP on "Embedded Systems & interfacing hands-on" 10th June 2019 to 14th June 2019.
- Two Week ISTE STTP Workshop on "CMOS Mixed Signal and Radio Frequency VLSIDesign" 30 Jan - 4 feb, 2017 at VNRVJIET, Hyderabad.
- One Week Workshop on Integrated Circuit and System Design using CAD tools" 12th – 17th June'2017.
- Maplesoft Product Overview- Level 1 with Maplesoft and Binary Semantics.
- A Two Day workshop on "FPGA Design Flow using VIVADO".
- Faculty Development Program on "Analog &Digital CMOS IC Design Flow Using Mentor Graphics EDA Tools" 19th-21st July 2012.

5. Academic Contribution and Research & Consultancy:

5.1. Invited Lectures:

5.2. Articles/Chapterspublished inBooks: Nil

5.3. Bookspublishedassingleauthororaseditor: Nil

5.4. Projects Guided:

a) UG:13

b) PG:03

5.5. Research Interests:

Low PowerVLSI design, VLSI System Design, Approximate Computing

5.6. Ph.D students: Nil

a) Enrolled:

b) Submitted:

c) Awarded:

5.7. Papers published in reviewed Journals:

S.No	Title of the Paper	Name of the Journal	ISSN / ISBN Number	Volume & Issue	Indexing
1	stacked keeper with body bias approach to reduce leakage power for 2-byte cam using 180nm cmos technology	7th IEEE-IACC-2017 Conference	Electronic ISSN**:** 2473-3571	10.1109/IACC.2017.0113	SCOPUS
2	design of a low power rom based logic (rbl) 4 bit multiplier using 180nm cmos technology	2nd international conference on signal processing, communications and system design	978 93 83038 42 8	2017	Google Scholar

5.8. Papers presented at National / International Conferences:

S.No	Title of the Paper	Name of the Journal	ISSN / ISBN Number	Volume & Issue	Indexing
1	Dual-threshold Single-ended Schmitt-Trigger Based Radiation Hardened memory Design with Fault modeling System	IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)	2319 – 4200	2017	Google Scholar
2	Power and Delay Analysis in Array Multipliers using Shorted gates FINFet based Full Adder	International Journal For Technological Research In Engineering	ISSN (Online): 2347 - 4718	Volume 2, Issue 12, August-2015	Google Scholar
3	Design And Implementation of Energy Efficient 4-Bit Binary CLA Based Incrementer/Decrementer Using Pass Transistor D Flip-Flop	International Journal For Technological Research In Engineering	ISSN (Online): 2347 - 4718	Volume 2, Issue 12, August-2015	Google Scholar
4	Design and Implementation of Low Power Dynamic Thermometer Encoder For Flash ADC	International Journal & Magazine of Engineering, Technology, Management and Research	ISSN No: 2348-4845	Volume No: 2 (2015), Issue No: 7 (July)	Google Scholar
5	Design and Implementation of 64-Bit Carry Select Adder in FPGA Technology	International Journal of Scientific Engineering and technology Research	ISSN 2319-8885 Pages:2423-2427	Vol.05, Issue.12, May-2016,	Google Scholar
6	Design of Efficient Multiplexer Based Encoder For Flash-ADC Using 120nm CMOS Technology	International Journal for Technological Research in Engineering	ISSN (Online): 2347 - 4718	Volume 2, Issue 12, August-2015	Google Scholar

5.9. Sponsored research Projects:Nil

5.10 Consultancy Projects:

S No.	Title	Agency	Period	Sanctioned Amount	Ongoing / Completed
1	Design and Development of 250 MHz SAR ADC	MMRFIC	1 Year	5 Lakhs	Ongoing
2	Design Of an FFT/IFFT IP-Core.	MMRFIC	6 Months	2 Lakhs	Ongoing

6. Awards / Honors received: Reviewer for IEEE Transactions on Very Large Scale Integration Systems

7. Motto: All power is with in you; you can do anything and everything, believe in that