Name : **K.SARATH CHNADRA**
Designation : Assistant Professor
Department :Electronics & Communication Engineering
Mail I.D: sarathchandra_k@vnrvjiet.in
Experience (in years): 10 years
Teaching: 11 years , Research: 5 years, Others (If any, Specify):

1.Educational/ Technical Qualifications.

S.No	Level	Year of passing	Specialization
1	Ph.D	pursuing	VLSI Design
2	M. Tech	2012	VLSI System Design
3	B.Tech	2008	Electronics& Communication Engineering
4	Intermediate	2004	M.P.C
5	SSC	2002	-

2.Teaching and Learning:

2.1.Teaching Interests:VLSI Design, Pulse and Digital Circuits, Analog Communications, Electronic devices & Circuits, Basic Electronics CMOS Analog IC Design, CMOS Mixed Signal IC Design, Electronic Circuit Analysis.

2.2. Novel Teaching & Learning Techniques adopted: WIT and WIL, Discussion Method, Brain storming, Mind mapping, POGIL

- Building some activities where students themselves find interest towards the topic by using different innovative concepts.
- Practical exercises were given to students in EDC and EC laboratory to make the students learn and build some amplifier circuits

2.3 Involvement in curriculum updating / Design: Program Assessment Member of M.Tech Program (VLSI System Design).Syllabus preparation of subjects like Digital System Design, Mixed signal for RFIC Design for R18 B.tech

3. Co-curricular and Extra-Curricular Activities

3.1. Interests and Hobbies: Developing Inter & Intra Personal Skills. Playing with kids and watching Television

3.2. CCA/ECA Organized: NA

3.3. CCA/ECA participated: Participated in Sports activities at VNRVJIET.

3.4. Counseling and Mentoring Activity: Mentoring for II, III & IV B.Tech ECE Students at VNR VJIET.

3.5. Committees involved in:
Department level: Member of Discipline committees VNRVJIET, Member ECE
Institute Level: Industry Institute Interaction Cell,Anti ragging, general discipline

4. Conference / Workshop / Seminar / Guest Lectures :

4.1 Conducted:

- Organised Webinar series on "RTL Design and Verification", 9th to 25 June 2020
- Co-ordinated Summar Course "VLSI Chip Design Hands on using Open Source EDA" E& ICT Acdemy IIT Guwahati at VNRVJIET, Hyderabad 08 – 12 July, 2019
- IEEE IACC 2017

4.2. Attended:

- Participated in two week Faculty development program on "Aspects of IC Design" conducted by Electronics & ICT Academy and Department of Electronics and Communication Engineering, NIT Warangal during 8th to 17th Feb, 2016.
- One Day Work Shop on "How to Write good Research Proposals", Feb 23 2018.
- NKN Summer Course-2019 on "Robotics & AI " NIT patna, from 24-28, June 2019
- Wireless and Mobile Communication, E& ICT NIT Warangal, 1st-6th July 2019.
- "Short term course on Introduction to Programming: A pedagogical approach" by E& ICT IIt Kanpur, 17th-21st June, 2019.
- "Python programming with Industry Perspective" E&ICT, NIT Patna, 2nd-6th Dec,2019
- One day session on "DFT and Verification" in IIIT Hyderabad, Feb,2020
- Webinar on "Teaching with Matlab in Modern Classroom" by IEEE hyd on April 16,2020
- Webinar on "Future Trends in CMOS Technology at 5nm and beyond" organized by chebrolu eng. College, Guntur. On 6th May 2020
- Webinar on "VLSI Design and Opportunities" delivered by Avinash Yadlapati and Organised by VNRVJIET on 30th May 2020.
- Work shop on Recent trends in signal processing, Antennae, VLSI and IOT organized by Sri Vasavi Engineering College, West Godavari 28th-30th May 2020.
- FDP "Advanced data structures, Organised by CSE,VNRJVIET, 1st to 11th June 2020.
- Faculty development program on "Art of Teaching" conducted by Enhance Edu IIIT, Hyderabad
- Faculty development program on "Designing of Digital circuits Using Synopsys Tools" by Seer Akademi, Hyderabad.

5 Academic Contribution and Research & Consultancy:

7.1.Invited Lectures:

- Delivered a Lecture on "Design of Sequential circuits" on the Occasion of certification course.
- Organized a series of webinars with support of Y. Padma sai, HOD-ECE on "RTL Design and Verification" from 9th june to 25th june2020.
- addressed the students about how VLSI evolved and challenges VLSI industry facing at present**.**

5.2. Articles/Chapters published in Books: NA

5.3. Books published as single author or as editor: NA

5.4. Projects Guided :

a) UG :12 Guided B.Tech projects in the areas of VLSI, Microcontrollers, and Embedded systems.

b) PG :8

5.5. Research Interests : Low Power VLSI, Physical Design, Analog IC Design

5.6. Ph.D students :

a) Enrolled :

b) Submitted:

c) Awarded:

5.7. Papers published in reviewed journals :

S.No	Title of the Paper	Journal Name Vol.No. PP	ISBN/ISSN No.	Impact Factor/ Citation Index	National/ International
1	Low Power and High Speed 4-Bit Flash Analog to Digital Converter Using Dynamic Latch Comparator Technique	International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Volume 4, Number 3 (2012), pp. 304-310	ISSN : 2278 – 8875	5.016	International
2	Design of 8T CNTFET SRAM for Ultra-Low Power Microelectronic Applications	IJRTE,Vol-8,Issue-4Nov-2019	ISSN: 2277-3878		International
3	Electrical Characteristics of Double Gate FINFET Under Different Modes of Operation	IJITEE,Vol-8,Issue-6S,April-2019	Online ISSN: 2278-3075 & Print ISSN: 0975-4350		International
4	CMOS Realization Of An Amplifier-Free Pipeline-Sar Adc Architecture For Low Power Applications	Jour of Adv Research in Dynamical & Control Systems	ISSN 1943-023X,Vol-10		International
5	CMOS Realization Of An Amplifier-Free Pipeline-Sar Adc Architecture For Low Power Applications	International Journal of Research and Analytical Reviews	e ISSN 2348 –1269, Print ISSN 2349-5138,Vol-5		International

5.8. Papers presented at National / International Conferences :

S.No	Title of the Paper	Names of the Conference/ Seminars	National/ International	Period
1	Design and Implementation of High Performance MIL-STD-1553B Bus Controlle	7th IEEE International Advance Computing Conference (IACC-2017)	International	5th-7th January 2017

5.9. Sponsored research Projects:

S.No	Title	Agency	Period	Grant amount	Ongoing / Completed

5.10 Consultancy Projects:

S.No	Title	Agency	Period	Sanctioned Amount	Ongoing / Completed
1	Design of MIL STD 1553 Remote terminal	Anant Technologies	2014	2,25,000/-	Completed

6. Awards / Honors received:

7. Motto: Live and Let Live