Name:**L.DHARMA TEJA**
Designation: Assistant Professor
Department: ECE
Mail ID: dharmateja _l@vnrvjiet.in
Experience (in years): 14.2 Teaching: 14.2 yrs Research: Others(if any, specify):

1. **Educational / Technical qualifications:**

S.No	Level	Year of passing	Specialization
1	Ph.D	pursuing	Low Power VLSI
2	M. Tech	2010	VLSI System Design
3	B.Tech	2006	Electronics& Communication Engineering
4	Intermediate	2001	M.P.C
5	SSC	1999	-

2. **Teaching and Learning:**

2.1.Teaching Interests: VLSI Design, Electronic Measurements and Instrumentation, Electronic Devices and Circuits, Pulse and Digital Circuits, Digital IC Applications, Principles of Communication, Digital Design through Verilog, Digital Logic Design, Analog Communications,CMOS Analog and Mixed signal IC design.

2.2. Novel Teaching & Learning Techniques adopted: WIT AND WIL, Discussion Method, Brain storming, Mind mapping, POGIL

2.3. Involvement in curriculum updating / Design: NA

3. Co-curricular and Extra-Curricular Activities

3.1. Interests and Hobbies

- Developing Inter & Intra Personal Skills.
- Gardening.
- Listening to music.

3.2. CCA/ECA Organized: NA

3.3. CCA/ECA participated: NA

3.4. Counseling and Mentoring Activity: 10 students from 1st year and 10 students from 4th year

3.5. Committees involved in:

Department level: NBA work,Class Review Comittee conduction for first and third year students ,File maintenence for comprehensive viva , Cultural fests, sports fest activities.

Institute Level: Post lock down preparation manual member for auditing ,Scintillations stage decoration committee member.

4.**Conference / Workshop / Seminar / Guest Lectures :**

4.1 Conducted:

- Organized four days TEQIP Sponsored workshop on “PCB Designing” in collaboration with TechnoTran, Hyderabad during 11th,12th,18th& 19th February 2016.
- Organized a three day workshop on “Concepts of Networking” in collaboration with Zonta Technologies, Hyderabad during 11thto 13th March 2014.
- Organized a ten days AICTE Sponsored workshop on “VLSI Design” in collaboration with EnhanceEdu by IIITH&VNR Vignana Jyothi Institute of Engineering & Technology, Hyderabad from 20th May 2013 to 1st June 2013.
- Organized a twelve days TEQIP Sponsored workshop on “Logical & Physical design Verification Using Verilog” inVNR Vignana Jyothi Institute of Engineering & Technology, Hyderabad from 1st April to 13th April 2013.
- Was a member in IACC 2017

4.2 Attended:

- Faculty development program on “Art of Teaching” conducted by Enhance Edu by IIIT Hyderabad.
- Faculty development program on "Designing of Digital circuits Using Synopsys Tools" by Seer Akademi, Hyderabad during 12th to 13th February, 2013.
- Attended a six month Pilot Program conducted by IGIP at BMS College of Engineering, Bangalore.
- Design of POGIL Activities for Outcome Based Education, Dept of EEE & IT,VNRVJIET from 9th -11th Dec 2014
- Effective English Communication Skills in September 2014
- 6 day FDP on CMOS, Mixed Signal and Radio Frequency VLSI Design by IIT Kharagpur, 10 week FDP on use of ICT in education for online and blended learning.
- Attended FDP on Art of Writing Papers and Research Methodologies at GRIET from 7th to 13th May 2020.
- Attended FDP on ‘Outcome Based Education and NBA Accreditation at Rajgads Dnyanpeeth’s Shri Chhatrapati Shivajiraje College of Engineering from 20th to 25th May 2020
- Attended FDP on Research Methodology at Rajgads Dnyanpeeth’s Shri Chhatrapati Shivajiraje College of Engineering from 12th to 17th May 2020.
- Attended FDP on Machine Learning and Artificial Intelligence at VNRVJIET conducted by ECE department from 8th to 12th June 2020.
- Attended FDP on Perspectives of Online Teaching And Learning at GRIET from 8th to 13th June.
- Attended FDP on Effective online Teaching using ICT Tools at VNRVJIET conducted by CSE department from 29th June to 4th July 2020.

5. Academic Contribution and Research & Consultancy:

5.1. Invited Lectures:

Delivered a Lecture on “HDL Programming Concepts” on the Occasion of 12-day short term course on “Logical & Physical design Verification Using Verilog” inVNR Vignana Jyothi Institute of Engineering & Technology, Hyderabad from 1st April to 13th April 2013.

5.2. Articles/Chapterspublished inBooks: NA

5.3. Books published as single author or as editor: NA

5.4. Projects Guided :

a) UG : 16 b)PG: 7

5.5. Research Interests : Low Power VLSI.

5.6. Ph.D students :

a) Enrolled :

b) Submitted:

c) Awarded:

5.7. Papers published in reviewed journals :

S.No	Title of the Paper	Journal Name Vol.No. PP	ISBN/ISSN No.	Impact Factor/ Citation Index	National/ International
1	Built-In-Self-Repair for Embedded RAMS with PMBIST or Efficient Fault Coverage	International Journal of Advances in	ISSN: 22311963	1.8896	International

		Engineering & Technology. Vol: 6, Issue:5 (2013), Page No: 2262-2273			
2	Study on Comparison of Various Multipliers	International Journal of Electronics and Communication Engineering & Technology Volume 4, Issue 5, September – October, 2013, pp. 132-142	ISSN 0976 – 6464(Print), ISSN 0976 – 6472(Online).	5.8896	International
3	Universal Modulator Using Cordic Algorithm For Communication Application	International Journal of Advances in Engineering & Technology Vol: 6, Issue: 6 (2014), Page No: 2480-2488	ISSN: 22311963	1.8896	International
4	Implementation of High Throughput Soft Output MIMO Detector Using PPTS Algorithm	International Journal & Magazine of Engineering & Technology, Management and Research.	ISSN: 23484845	1.74	International Journal
5	Design of Low Power SRAM Cell Using Multi Threshold Technique	Advanced Science Letters	E-ISSN:1936-7317	0.20	International Journal
6	"Design of High Performance 4-Bit Ternary Multiplier using CNTFET"	International Journal of Innovative Technology and Exploring Engineering (IJITEE)	ISSN: 2278-3075	6.03	International Journal
7	"Review of Design and Analysis of Different Technologies in Low Power VLSI Circuits"	Science, Technology and Development	ISSN:0950-0707	6.1	International Journal

5.8. Papers presented at National / International Conferences :

S.No	Title of the Paper	Names of the Conference/ Seminars	National/ International	Period
1	Design of SRAM Using Hetero Junction Tunneling Transistors and Comparing With CMOS Design	4th International Conference on 'Computing, Communication and Sensor Network',CCSN2015.	International	Feb, 2016, Kolkatta, India

5.9. Sponsored research Projects:

S.No	**Title**	**Agency**	**Period**	**Grant amount**	**Ongoing / Completed**

5.10 Consultancy Projects:

S.No	**Title**	**Agency**	**Period**	**Sanctioned Amount**	**Ongoing / Completed**

6 Awards / Honors received:

7 Motto: At the end of day, before you close your eyes, be content with what you have done and be proud of whom you are.

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