Name: **J.L.V.RAMANA KUMARI**
Designation:Assistant Professor
Department: Electronics & Communication Engineering
Mail ID: ramanakumarijasty@gmail.com
Experience (in years):Teaching:16 Research: Others (If any, Specify):

1. Educational / Technical qualifications:

S.No	Level (UG / PG / Ph.D)	Year of passing	Specialization
1	Ph.D	Pursuing	VLSI Testing
2	M.Tech	2009	VLSI System Design
3	B.Tech	1991	ECE

2. Teaching and Learning:

2.1. Teaching Interests:
Computer organization, Switching Theory and Logic design, CPLD & FPGA, VLSI Testing , Design For Testability, Algorithms For VLSI Design ,Digital System Design.

2.2. Novel Teaching & Learning Techniques adopted:
Videos, POGIL,PPT, Group Discussion

2.3. Involvement in curriculum updating / Design:
Updating the syllabus of subjects VLSI, DSD, DFT, AVDA , HDL base design and Verification etc.

3. Co-curricular and Extra-Curricular Activities

3.1. Interests and Hobbies:Reading books, listening to music, shopping, Cooking.
3.2. CCA/ECA Organized: Arranged open house project in convergence of 2015
3.3. CCA/ECA participated: Posters presentation in convergence 2015
3.4. Counseling and Mentoring Activity: Mentoring I,II, III and IV B.Tech students
3.5. Committees involved in:

Department level:

- Coordinator for Mini Projects of M.Tech (VLSI System Design).
- Project-coordinator for Major Projects of M.Tech (VLSI System Design)
- Counseling and Mentoring Activity: Mentoring II, III and IV B.Techstudents, Counseling M.Tech students when required.
- Journal Publications File coordinator

Institute Level:

- Anti-ragging Committee
- CCA Activities
- Admissions
- Teachers association member

4. Conference / Workshop / Seminar / Guest Lectures:

4.1.Conducted:

- Full-custom IC Design and FPGA Design flow at VNRVJIET ON 23rd to 25th February'2012.
- Training program on "Logical and physical design of digital circuits using HDL and Mentor Graphics Tools" from01.04.2013 to 13.04.2013.
- Short term course on "Design of digital circuits using Verilog" for 30 days from 21.03.2013.
- Faculty development program conducted on VLSI Design from 20.05.2013 to 01.06.2013
- Training program on logical & Physical design of digital circuits using Synopsys Tools from 09.12.2013 & 10.12.2013.
- "Training on Synopsys tools" was organized on 05.04.2014 by Sri. M. Shiva Kumar,

Senior Manager, AMD Research and Development Center India Pvt. Ltd, Hyderabad. At VNRVJIET,ECE Department.

- "Training on Synopsys tools" was organized on 26.12.2014 and 27.12.2014 by Sri Achinth Vats Application Engineer, Eigen Technologies, New Delhi at VNRVJIET, ECE Department
- TEQIP-II sponsored Guest lecturer on "MEMS ,RF circuits and Circuit level Design in industries" by Invited Professor Shiban K.Koul ,Deputy Director(S&P) and Professor ,Centrs for Applied Research in Electronics, IIT(Delhi) on 17.07.2015
- TEQIP-II Sponsored Training program on VLSI Desin Flow and Hardware Implementation from 27.07.2015 to 07.08.2015 at VNRVJIET ,ECE Dept.
- Guest lecturer on HDL based Design using System Verilog on 11.12.2015 by N. Madhu Sudan Reddy ,Designer Engineer, CYIENT, Hyderabad.
- Guest lecturer on HDL based Design Verification using System Verilog on 21.01.2016 by N. Madhu Sudan Reddy ,Designer Engineer, CYIENT, Hyderabad
- Guest lecturer on Design for Testability on 19.03.2016 by Anand S Moghe Sr. manager Xilinx Hyderabad .
- Conducted Two Day work-shop on PCB Design in 24 and 25th March'2017 at VNRVJIET.
- Integrated circuit and System Design using CAD Tools "A one week workshop from 12.06.2017 to 17.06.2017 at VNRVJIET.
- Conducted Guest lecture and Interaction on "" Career opportunities for Freshers in VLSI industry"" by D.Yadagiri. Design Verification Engineer, AMD for M.Tech II Year VLSI and ES students.29.08.2020
- Conducted Interactive session for M.Tech VLSI & ES Students with D.Srikanth ,Sr staff Engineer, Xilinx, Hyderabad. On 19.12.20 for intern ships and placements

4.2. Attended:

- Embedded Systems March 2006.
- Teaching Methodologies. May 2007.
- Ist International Student Track on VLSI Design Signal processing and Wireless protocol Development. In Jan'2008
- XILINX Technology Workshop on Digital Design with FPGA Dec'2008.
- Muffakham Jah College of Engineering and Technology a one day tutorial on mixed signal VLSI Design on 24th December '2011.
- International conference on 9thand 10th Jan 2012 on VLSI Design & embedded systems at HITEX.
- Free seminar on VLSI Design on 6th March'2012at Taj Deccan organized byJNTUH & CADENCE.
- "E-CAD & VLSI DESIGN" Workshop at "Mahatma Gandhi Institute ofTechnology" from 06.09.2012 TO 08.09.2012 on
- Faculty development program on Analog System Design Using TI ASLKv2010 from 14th -16th Feb-2013 at VNRVJIET.
- Work shop on Research methodologies 02.02.2013 & 09.02.2013 at IIIT, Hyderabad.
- Work shop on ART OF TEACHING 02.05.2013 to 04.05.2013
- POGIL workshop on 14.05.2013
- Attended 6 Day workshop on "Research Methodology" at JNTUH from 16.12.2013 to 21.12.2013
- Coreel university program (CUP) titled "Zynq located on Zed Board using Vivado and IP Integrator "on 20.01.2014 at Coreel Technologies, Hyderabad.

- "synopsys training program"from 11.06.2014 to 13.06.2014 & 16.06.2014 to18.06.2014at Synopsys , DivyaSree Omega, Block B, Hitech City Main Road, Kothaguda, Hyderabad
- "Training on Synopsys tools" was attended from26.12.2014 to 27.12.2014 by Sri Achinth Vats Application Engineer, Eigen Technologies, New Delhi at VNRVJIET, ECE Department.
- Attended Guest Lecture on "A Developer's Perspective of Becoming anEmbedded and VLSI System Expert ", by Mahesh U Patel, Principal TechnicalOfficer, C-DAC, Hyderabad on 06-06-2015.
- TEQIP-II sponsored Training program on VLSI Desin Flow and Hardware Implementation from 27.07.2015 to 07.08.2015 at VNRVJIET ,ECE Dept
- TEQIP-II sponsored Three-day national level workshop 28 to 30 Jan 2016on "Research in Innovations" conducted by CSE Dept ,VNRVJIET.
- Two Week ISTE STTPWorkshop on "CMOS Mixed Signal and RF VLSI Design" 30 Jan - 4 Feb, 2017 at VNRVJIET, Hyderabad.
- One week Faculty awareness program on "Contemporary research and IPR" from 28.01.2019 to 01.02.2019 at JNTUH.
- Online workshop on scientific writing for Journals organized by springer nature 20.05.2020.
- Three Day National Level Online Faculty Development Program on "Research Trends in Signal Processing, Antennae,VLSI & IoT" during 28th -30th May 2020, Organized by The Department of Electronics & Communication Engineering, Sri Vasavi Engineering College(Autonomous)Tadepalligudem,Andhra Pradesh 534101.
- Three Day Faculty Development Program on VLSI Design Flow from 28.05.2020 to 30.05.2020 hosted by Dept of ECE Anurag University in association with Institution of Engineers(IEI) and Entuple technologies.
- Five Day ATAL Faculty Development Program Internet Of Things from 31st M to 4th June conducted by JNU New Delhi India
- Five DAY Online FDP Artificial Intelligence and Machine Learning for engineering Applications conducted during 8th -12th June '20202 by the departments of CSE,IT & ECE.
- Online workshop on "DATA SCIENCE:TECHNIQUES &TOOLS " conducted by MITS GWALIOR from 20th -21st June'2020
- AICTE sponsored Short Term Training Program (Slot 2) on "Machine learning and Deep learning models for Medical domain applications" from October 19th to 24th 2020, Manipal Institute of Technology.
- attended the AICTE Training and Learning Academy (ATAL) sponsored One Week Online Faculty Development Programme on "Design Thinking" from 8th-12th November 2020, organized by Department of Mechanical Engineering, Sri Manakula Vinayagar Engineering College (Autonomous Institution) Madagadipet, Puducherry.
- Two Week AICTE Sponsored Online Faculty Development Programme (FDP) on "Recent Trends in VLSI Design, Signal Processing & Optimization based on EDA tools" 7th to 19th Dec 2020
- Attended Webinar "VLSI-Physical Design Using Mentor Graphics EDA Tools " By CoreEl Technologies By B.Nagendra on 28.01.2021
- Attended webinar State of the art silicon VLSI:Industrial Face of Nanotechnology By Dr.Michael shur on June 01,2021

5. Academic Contribution and Research & Consultancy:

5.1. Invited Lectures:

Resource person to give Lecture on Spice, DA-IC backend tool flow in in FDP ON VLSI Design Conducted During May'2013.

5.2. Articles/Chapterspublished inBooks: NIL

5.3. Bookspublishedassingleauthororaseditor: NIL

5.4. Projects Guided:

a) UG: 18

b) PG: 14

5.5. Research Interests: VLSI Testing.

5.6. Ph.D students: Nil

a) Enrolled:

b) Submitted:

c) Awarded:

5.7. Papers published in reviewed Journals:

5.8. Papers presented at National / International Journals/ conferences:

S.No	Title of the Paper	Names of the Journals /	National/ International	Period	
1.	Diagnosis Of Alzheimer's Disease Using Cnn Approaches	Journal of Biological Engineering Research and Review	International	December'2021 ISSN: 2349-3232	-
2.	3-cell NPSF Testing In Memories Using Hamiltonian and Gray Sequence	Journal of Computational and Theoritical Nanoscience	International	Nov'2020	Scopus
3	FPGA Implementation of Testing Active NPSF using Tiling Method	IJITEE	International	Nov-2019	Scopus
4	NPSF Testing using Block Code Technique	Global Journal of Computer Science and Technology, 2018	International	2018	
5	FPGA Implementation of NPSF Testing using Block Code Technique	Global Journal Of Science and Technology	International	2018	peer-reviewed journal
6	FPGA Implementation of Decimal Frequency Divider using 12C	CiiT Programmable Devices and circuits and Systems	International	2018	Vol-2

7	Design Verification and test vector Minimization Using Heuristic Method of A Ripple Carry Adder	International Journal on Cybernetics & Informatics (IJCI)	International	Vol. 5, No. 4, August 2016	Open access peer-reviewed journal
8	Test Minimization For Full Adder Using Integer Linear Programming And DFT Tools	International Journal of Recent Advances in Engineering & Technology (IJRAET	International ISSN (Online): 2347 - 2812	3rd and 4th July ,2015 at MRECW	1.75
9	FPGA Implementation of High Speed Test Pattern Generator for BIST	IJERT	2278-0181 Vol 2	Nov 2013	1.76
10	Low voltage. Low Power, SRAM Design on Schmitt Trigger Technique	IOSRJVSP	2319-4200 Vol 3	Nov 2013	1.645
11	FPGA Implementation of Counter By using State Look Ahead Logic	IJERA	2248-9622 Vol 2	June- July 2012	1.76
12	Physical Design of Memory and Detection of Stuck-At-Fault	IJERA	2248-9622 Vol 2	July-August 2012	1.76

5.8.a Papers presented at National / International Conferences:

S. No	Title of the Paper	Names of the Conference/ Seminars	National/ International	ISBN/ISSN	Period
1.	Power Optimization Analysis Of Different Sram Cells Using Transistor Stacking Technique	IEEE	International	978-1-6654-0962-9/21/$31.00 ©2021 IEEE	Nov-2021

2	Testing Of Neighborhood Pattern Sensitive Faults For Memory	ICSCSP-2020	International		2020, Aug-20-21
3	FPGA implementation of test vector monitoring BIST architecture system	ICMEET	International	CrossRef Metadata Search DOI: 10.1007/978-81-322-2728-1_67	2017
4	FPGA Implementation of Memory Design And Testing	IEEE Conference	International		05.01.2017 to 07.01.2017
5	FPGA Implementation Memory Design And Testing	IEEE Conference	International	2473-3571	Jan'5th to 7th
6	FPGA Implementation of Test Vector monitoring BIST Architecture System	International Conference On Microelectronics,Electromagnetics and Telecommunications[ICMEET-2016]	International Conference	DOI 10.1007/978-81-322-2728-1_67	18th&19th Dec'2015 GITAM University, Vishakhapatnam
7	Test Minimization For Full Adder Using Integer Linear Programming And DFT Tools	International Conference On Signal Processing , Communications and System Design [ICSPCOMSD-2015	International	ISSBN:978-93-83038-33-6	3rd and 4th July ,2015 at MRECW
8	Fault based Test minimization for digital circuits using integer linear	National conference on VLSI, Signal Processing and Embedded Systems(Velasi-Em-2012),VNR Vignana Jyothi Institute of Engineering and	National		Aug 2012

	programming and design for testability	Technology,Hyderabad,India.			
9	FPGA Implementation of Modified Genetic Algorithm for Fourphase Code Design	National Conference NCIS-2010	National		23rd& 24th April
10	Four Phase code Design Using Modified Genetic Algorithm	National Conference on emerging Trends in RF Signal processing FISAT	National		25th - 27thMar'2010

5.9. Sponsored research Projects:

S.No	Title	Agency	Period	Grant amount	Ongoing / Completed

5.10 Consultancy Projects:

S.No	Title	Agency	Period	Sanctioned Amount	Ongoing / Completed

6. Awards / Honors received:

- Best project award for M.Tech Project "FPGA Implementation Test vector Monitoring BIST Architecture System." in 2015
- Best project award for M.Tech Project"FPGA Implementation of High Speed Test Pattern for BIST" in 2013
- Judge For the Event E-PAPYRUS 11,12-Mar'2015 at JNTUH
- Best project award for M.Tech Project "FPGA Implementation Of Testing of NPSF in memories using tiling Method." in 2019

7. Motto: Go confidently in the direction to fulfill the dream.