

Name : **Dr. Aruru Sai Kumar**
 Designation : Assistant Professor
 Department : Electronics & Communication Engineering
 Mail I'd : saikumar_a@vnrvjiet.in
 Experience (in years): 11.5
 Teaching: 7.5 Years Research: 4 Years Others(if any, specify): Nil



1. Educational / Technical qualifications:

S.No	Level (UG / PG / Ph.D)	Year of passing	Specialization
1	Ph.D	March 2022	VLSI Design
2	M.Tech	2010	VLSI Design
3	B.Tech	2008	ECE
4	Intermediate	2004	MPC
5	SSC	2002	----

2. Teaching and Learning:

2.1. Teaching Interests:

Switching Theory and Logic Design, VLSI Design, Digital Design Through Verilog HDL, Low Power VLSI Design, CPLD & FPGA Architectures & Applications, MPMC, Signals and Systems, Control Systems, Embedded Systems.

2.2. Novel Teaching & Learning Techniques adopted: POGIL, WIT & WIL and Learning by Doing.

2.3. Involvement in curriculum updating / Design:

3. Co-curricular and Extra-Curricular Activities

3.1. Interests and Hobbies: Listening Music and Playing cricket

3.2. CCA/ECA Organized:

3.3. CCA/ECA participated:

3.4. Counseling and Mentoring Activity: Yes

3.5. Committees involved in:

Department level:

Institute Level:

4. Conference / Workshop / Seminar / Guest Lectures :

4.1 Conducted: Nil

4.2 Attended: 11

- A three day work shop on MATLAB conducted by iMatrix Technologies in Regency Institute of Technology during 9th -11th August 2010.
- Faculty Development Program on "Exploring for Excellence in Education" at MLRITM on 26th Nov. 2015 and the speaker is Prof. M L Sai Kumar.
- Faculty Development Program on "VLSI System Design" at MLRITM on 28th Nov 2015 and the speaker is Dr. Rahul Shreshta (Asst. Prof. IIIT Hyderabad).
- One day FDP for MLRITM faculty on "Technical Paper Writing Using LaTeX" by Dr. Srinivas Nallagonda on 17th March 2017.
- One week workshop on "Internet of Things (IoT)" by Dr. B. Lakshmi, during 08th -13th May, 2017 in NIT Warangal (TEQIP).
- One week Faculty development programme on "Fundamentals of Signals, systems and random variables with hands-on session using MATLAB", during 5th June to 10th June 2017 in Geethanjali College of Engineering and Technology.
- One week Faculty development programme on "Advanced CMOS VLSI" from 3rd to 8th December 2018 organized by E&ICT academy, NIT Warangal.

- One week Faculty development programme on "Nanoscale Devices and Circuits" from 17th to 22nd June 2019 organized by E&ICT academy, NIT Warangal.
- One week Faculty development programme on "Biomedical Signal Processing" from 11th to 16th December 2019 organized by E&ICT academy, NIT Warangal.
- A 5-day short term training program (STTP) on "Electronics Systems: Devices, IC and Applications" organized by Department of Electronics and Communication Engineering, NIT Arunachal Pradesh from 14th–18th March 2022 in online mode, sponsored by AICTE.
- Eight day FDP on "Introduction to Low Power VLSI Design and Applications" from 23rd December to 03rd January 2022 organized by E&ICT academy, NIT Warangal.

5. Academic Contribution and Research & Consultancy:

5.1. Invited Lectures: Nil

5.2. Articles / Chapters published in Books: Nil

5.3. Books published as single author or as editor: Nil

5.4. Projects Guided :

a) UG : 12

b) PG : 03

5.5. Research Interests : Network-on-Chip (NoC) architecture design, Application Core Mapping in 2-D

and 3-D environments, Fault Tolerant Network-on-Chip and Low Power VLSI Design.

5.6. Ph.D students :

a) Enrolled : 01 (Part-Time, LPU University)

b) Submitted : Nil

c) Awarded : Nil

5.7. Papers published in reviewed journals : 10

S.No	Title of the Paper	Name of the Journal	ISSN / ISBN Number	Volume & Issue	Indexing
1	An Efficient Real - Time Embedded Application Mapping For NoC Based Multiprocessor System on Chip	Wireless Personal Communications (Springer)	e-ISSN: 1572-834X	2022	Science Citation Index Expanded (SCIE)
2	Performance and Communication Energy constrained Embedded Benchmark for Fault Tolerant Core Mapping onto NoC architectures	International Journal of Ad Hoc and Ubiquitous Computing (Inderscience Publishers) (Impact Factor-0.654)	ISSN online 1743-8233	2022	Science Citation Index Expanded (SCIE)

3	Performance Assessment of Adaptive Core Mapping for NoC-based architectures	International Journal of Embedded Systems (Inderscience Publishers) (Impact Factor-1.2)	ISSN 1741-1076	2022	Emerging Sources Citation Index (ESCI), Scopus (Elsevier)
4	An Adaptive Core Mapping Algorithm on NoC for Future Heterogeneous System-on-Chip	Computers and Electrical Engineering (Elsevier) (Impact Factor-3.818)	ISSN: 0045-7906	Vol 95, 2021	Science Citation Index Expanded (SCIE)
5	Evaluation of low power consumption network on chip routing architecture	Microprocessors and Microsystems (Elsevier) (Impact Factor-1.525)	ISSN: 0141-9331	Vol 82, 2021	Science Citation Index (SCI)
6	Scalable benchmark synthesis for performance evaluation of NoC core mapping	Microprocessors and Microsystems (Elsevier) (Impact Factor-1.525)	ISSN: 0141-9331	Vol 79, 2020	Science Citation Index (SCI)
7	Implementation of High speed and Low power 6T SRAM cell using FinFET at 22nm technology	International Journal of Engineering And Computer Science	ISSN: 2319-7242	Vol. 5, No. 12, 2016	Web of Science (WoS)
8	Development of effective method for agriculture monitoring using WSN and IOT	International Journal of Research (IJR)	e-ISSN: 2348-6848	Vol 2, Issue 8, 2015	UGC CARE LIST
9	Analysis for saturation throughput using various mechanisms for IEEE 802.11 WLAN's	International Journal For Research in Applied Science and Engineering Technology	ISSN: 2321-9653	Vol. 2, No. 5, 2015	Scopus
10	A Robust Algorithm For Digital Image Copyright Protection	International Journal of Electrical and Electronic Engineering & Telecommunications	ISSN 2319 – 2518	Vol. 3, No. 3, 2014	UGC CARE LIST

5.8. Papers presented at National / International Conferences: 04

S.No	Title of the Paper	Names of the Conference/ Seminars	National/ International	Period
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1	An efficient and flexible AI based customized platform for online	International Conference on Cognitive & Intelligent Computing (ICCIC-21), India.	International	2022
2	An efficient low latency router architecture for mesh based NoC	International Conference on Communications, Signal Processing and VLSI (IC2SV-2019), NIT Warangal.	International	2021
3	Exact Formulas for Fault Aware Core Mapping on NoC Reliability	2020 IEEE 17 th India Council International Conference (INDICON-2020), New Delhi, India.	International	2020
4	Efficient Core Mapping on Customization of NoC Platforms	2019 IEEE International Symposium on Smart Electronic Systems (iSES-2019) (Formerly iNiS), NIT Rourkela, India.	International	2019

5.9. Sponsored research Projects: Nil

S.No	Title	Agency	Period	Grant amount	Ongoing / Completed

5.10 Consultancy Projects: Nil

S.No	Title	Agency	Period	Sanctioned Amount	Ongoing / Completed

6. Awards / Honors received:

- UGC-NET (Assistant Professor) Qualified in June-2014, December-2014.
- GATE-2010, GATE- 2014, GATE-2017 Qualified.
- Member of IEEE (Member ID-96332046), Hyderabad Section.
- Life Member of IETE (M-502917).
- Reviewer of the following journals
 - Microprocessors and Microsystems
 - Silicon
 - International Journal of Ad Hoc and Ubiquitous Computing
 - International Journal of Embedded Systems

7. Motto: There are no shortcuts to Success, it is the result of Preparation, Hard work and Learning from Failures.