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# VALLURUPALLI NAGESWARA RAO VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY



## Department of Electronics and Communication Engineering

### M.Tech-VLSI System Design

#### About the Programme

**Master of Technology in VLSI System Design** is a two-year post graduate programme dedicated to enlightening students with the designing, implementing and testing of the VLSI IC to make it viable, maintainable, and affordable. The programme offer students with a strong base of VLSI principles and applications in scientific and engineering domains.

- ❖ Started in the year **2003 with an intake of 18**
- ❖ Accredited by **NBA in 2015**
- ❖ No. of Batches Graduated: **18**
- ❖ No. of Faculty with VLSI specialization :**20**  
(30% of total Department faculty)
- ❖ No. of Ph.D faculty with VLSI specialization: **06**
- ❖ No. of Collaborations with VLSI industries: **13**
- ❖ Placements: **100% (Out of which 80% in core industries)- Highest Package – 24 Lakh**
- ❖ No of students associated in Consultancy and Sponsored projects: **Minimum 3 from batch**
- ❖ IEEE collaborations: **Circuits and Systems Society Student Chapter established in 2020**

#### Future Areas in VLSI

- ❖ **Low power VLSI**
- ❖ **Digital IC Design**
- ❖ **Analog IC Design**
- ❖ **Mixed & RFIC Design**
- ❖ **Design For Testability**
- ❖ **Device Modeling**
- ❖ **System Design using FPGA**
- ❖ **Machine Learning in VLSI**
- ❖ **VLSI for Biomedical Applications**
- ❖ **VLSI for Wireless Communication**
- ❖ **VLSI for IOT**
- ❖ **Nano Technology**

#### Placements

100 % Placements

Highest Package 14 Lakhs per Annum

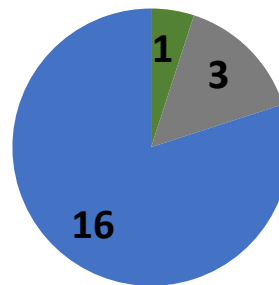
Qualcomm

NOSCHIP

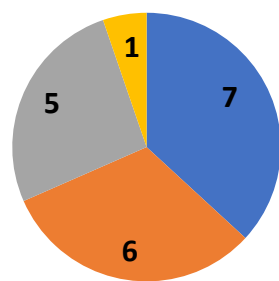


SYNOPSYS®

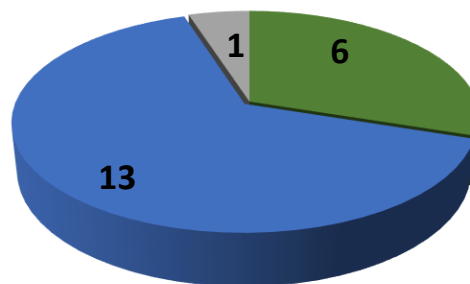
#### Faculty Strengths



■ PROFESSORS  
■ ASSOCIATE PROFESSOR  
■ ASSISITANT PROFESSOR



■ MORE THAN 15YEARS  
■ 10-15YEARS EXPERIENCE  
■ 5-10 YEARS EXPERIENCE  
■ <5 YEARS EXPERIENCE



■ FACULTY WITH Ph.D  
■ FACULTY PURSUING Ph.D.  
■ FACULTY WITH M.Tech

#### Collaborations with Industry

##### Training Programs offered in collaboration with Industry

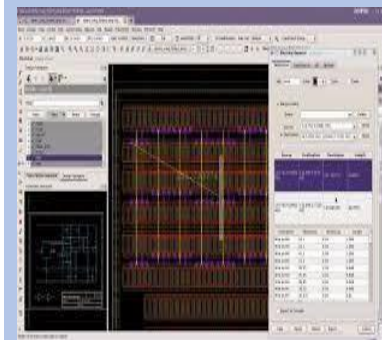
- ❖ **ASIC Design using Synopsys**
- ❖ **Full Custom Design using EDA tools**
- ❖ **RTL Design and Verification**
- ❖ **FPGA Implementation using VIVADO**
- ❖ **Advanced Digital Design and Verification using System Verilog HDL**



#### Tools Available



- ❖ **Synopsys (Front End & Back End University Bundle)**
- ❖ **Mentor Graphics (Front End & Back End Tool)**
- **Xilinx Vivado System Edition**



FPGA KITS