Name: **Kattekommula Swetha Reddy**
Designation: Assistant Professor
Department: Electronics and Communication Engineering
Mail.I.D: swethareddy_k@vnrvjiet.in
Experience (in years): Teaching: 6 yrs Research: 00 Others (Industry):1.5 yrs

1. Educational / Technical qualifications:

S.No	Level	Year of passing	Specialization
1	Ph.D	pursuing	VLSI Design
2	M. Tech	2014	VLSI System Design
3	B.Tech	2012	Electronics& Communication Engineering
4	Intermediate	2008	M.P.C
5	SSC	2006	-

2. Teaching and Learning:

2.1.Teaching Interests:

Digital System Design, MOS Circuits, VLSI Design, Simulation and synthesis of PLDs, VLSI Design Verification and Testing, Low Power VLSI, Physical Design Automation, Scripting languages like PERL, TCL for VLSI, CPLD & FPGA Architectures and Applications, Design for Testability, Programming through C, ASIC Design, Digital IC Design, Python Programming.

2.2.Novel Teaching & Learning Techniques adopted:

Active Learning Techniques like Think Pair Share, Mentimeter, Clickers and plickers, Online courses through NPTEL, Spoken Tutorial, POGIL, PPTs, Videos, Chalk and Talk, WIT & WIL etc.

2.3. Involvement in curriculum updating / Design:

- M Member of Programming Assessment committee (PG-VLSI System Design) for R18 regulation in 2018.
- Syllabus preparation of subjects like Digital System Design, Verification and Scripting Languages for VLSI Design, ASIC Design for R18 B.tech.

3. Co-curricular and Extra-Curricular Activities

3.1. Interests and Hobbies:

Gardening, reading Novels, exploring internet for recent trends in technology.

3.2. CCA/ECA Organized:

3.3. CCA/ECA participated:

- Visited R & D showcase in IIIT Hyderabad, Feb18,2017
- Participated in Rally for " Anti-drug campaign" by NSS VNRVJIET in 2018.
- Visited IIT Madras for "SARAANG Fest Program", Chennai, Jan 2020
- Co-ordinated First Year Student Induction Program in 2020
- Industrial Visits to Ananth Technologies Pvt. Ltd, ICOMM, INCOIS, SCL Sulakshana Circuits Ltd and L&T metro station (UPPAL control office).
- Actively involved and participated in sintillashunz-2022 (National Level fest) in VNRVJIET.

3.4. Counselling and Mentoring Activity:

- Mentored 24 B.Tech (2016 batch) Students.
- Mentoring 10 B.Tech (2020 batch) Students.

3.5. Committees involved in:

Department level:

- Revenue Generated from industrial training file incharge for NAAC 2018.
- Class Co-ordinator of 2020-2024 B.Tech ECE-C.

- Member of Project Review committee for IV B.Tech VLSI Design SIG.
- Member of Project Review committee for M.Tech VLSI Design.
- Member of Special Interest Group – VLSI.
- Department Budget File incharge from 2019 onwards.
- IV B.Tech ECE Project File incharge.
- SPOC for Student data Maintenance of ECE.

Institute Level:

- Member of OTLE(Online Teaching, Learning and Evaluation) Committee from 2020 onwards.

4. Conference / Workshop / Seminar / Guest Lectures:

4.1. Conducted:

1. FDP Workshop on Integrated Circuit and System Design using CAD Tools, 14^{th} - 17^{th} June 2017
2. Co-ordinated Summer Course "VLSI Chip Design Hands on using Open source EDA" E& ICT Academy IIT Guwahati at VNRVJIET, Hyderabad 08^{th} – 12^{th} July, 2019
3. Organised Webinar series on "RTL Design and Verification", 9^{th} to 25^{th} June 2020
4. Co-ordinated NIT Patna based Joint FDP on "Embedded UVM Open Source Emulation & Functional Verification" from July 13^{th} - July 24^{th}, 2020
5. Co-ordinating VLSI Training for B.tech II Year II sem ECE in May and June, 2021

4.2.Attended:

1. Workshop on "Low Power Embedded Systems using ARM Cortex-M4F based MSP432" 16^{th} – 18^{th} June 2016 at VNRVJIET, Hyderabad.
2. ITRA Sponsored 4 Day National Level Workshop on "Bio-Medical Signal Processing & Its Applications" 13^{th}-16^{th} Dec 2016
3. Two Week Workshop on "ISTE STTP CMOS Mixed Signal and Radio Frequency VLSI Design" in Association with IIT, Kharagpur. 30^{th} Jan to 4^{th} Feb 2017
4. Workshop on "IOT and Embedded Systems" 20^{th} - 21^{st} Feb 2017,
5. FDP workshop on "Recent Trends in signal Processing and its applications", 22^{nd} June - 1^{st} July 2017.
6. 20-Day workshop on "Pandit Madan Mohan Malaviya National Mission on Teachers and Teaching Induction Training Programme", 28^{th} Nov – 20^{th} Dec 2017 at IIT Bombay.
7. One Day Work Shop on "How to Write good Research Proposals", Feb 23^{rd} 2018.
8. NKN Summer Course-2019 on "Robotics & AI " NIT patna, from 24-28, June 2019
9. Wireless and Mobile Communication, E& ICT NIT Warangal, 1^{st} July to 6^{th} July 2019.
10. "Short term course on Introduction to Programming: A pedagogical approach" by E& ICT IIt Kanpur, 17^{th}-21^{st} June, 2019.
11. "Python programming with Industry Perspective" E&ICT, NIT Patna, 2^{nd} Dec to 6^{th} Dec,2019
12. One day session on "DFT and Verification" in IIIT Hyderabad, Feb,2020
13. Webinar on "Teaching with Matlab in Modern Classroom" by IEEE Hyd on April 16^{th} ,2020

14. One week ATAL FDP on “Artificial Intelligence to career enrichment”, 27th April – 2nd May 2020.
15. Webinar on “Future Trends in CMOS Technology at 5nm and beyond” organized by chebrolu eng. College, Guntur. On 6th May 2020
16. Webinar on “VLSI Design and Opportunities” delivered by Avinash Yadlapati and Organised by VNRVJIET on 30th May 2020.
17. Work shop on Recent trends in signal processing, Antennae, VLSI and IOT organized by Sri Vasavi Engineering College, West Godavari 28th-30th May 2020.
18. FDP "Advanced data structures, Organised by CSE, VNRJVIET, 1st to 11th June 2020.
19. 3-Day FDP on “Effective Utilization of Digital Platforms for Content Development and Delivery” by IIT Bombay, VNRVJIET from 13th-15th July 2020.
20. One- week PDP on “NBA in a Nutshell” organised by VNRVJIET from 27th July to 1st August 2020.
21. Webinar on ““Pitfalls of IP Power estimation for AI and vision SoCs and how to avoid them” by Synopsys on 23rd July, 2020
22. Webinar on “High- Speed Serdes PHY-IP for upto 800G hyper-scale data centers.” On August 4th, 2020
23. Webinar on “Recent Trends and Challenges in VLSI Fabrication Technology” on 8th August 2020.
24. Webinar on “Accelerate Low Power Static Verification with New Technologies” from Synopsys by Sara Li, Application Engineer, on 11-08-2020
25. Webinar on “GPU-Powered SPICE: The Way Forward for Analog Simulation, by Chen Zao, AEM, Empyrean Software on 12-08-2020
26. Webinar on Using the Virtual Prototype of the S32G Safe and Secure Vehicle Network Processor on 19th August 2020
27. Webinar launch of Digital AI lab by Idea labs on 20th August 2020.
28. Webinar on “Industry oriented VLSI Design and Verification” 21st August 2020.
29. Joint FDP on “Demystifying 5G RF ASICs” by IIT Guwahati & NIT Patna 24th august to 4th September 2020.
30. National Workshop on “Technical writing and presentation with Latex” 29th and 30th of August 2020.
31. Joint FDP on “Python Programming” by IIT Kanpur, NIT Patna from 7-09-2020 to 19-09-2020.
32. Joint FDP on “Digital Tools for Writing, Authoring, Reviewing” by NIT Patna from 21st September -2nd October 2020.
33. Five Day ATAL FDP on Applied Data Science organizing by the University College of Engineering, JNTUK, Kakinada during 5th-9th October 2020.
34. FDP on AICTE sponsored Short Term Training Program (Slot 2) on “Machine learning and Deep learning models for Medical domain applications” from October 19th to 24th 2020.
35. FDP on “Mathematics for DATA Science” by CSE, VNRVJIET.27th-31st October 2020.
36. ATAL FDP on “Design Thinking” from 8th -12th Nov, 2020
37. FDP on Python Basics by VNRVJIET” from 9-12 Nov 2020
38. FDP on “Recent Trends in VLSI Design, Signal Processing Optimization of EDA tools” (7th Dec to 19th Dec 2020)

39. FDP on AMPLE on 20th, 21st & 22nd Jan 2021.
40. PDP on "Introduction to Data structures for AI" 22nd Feb 2021 to 8th April 2021
41. IEEE Webinar on "Become the authentic Leader-your Envision" on the occasion of International Women's Day" on Mar 8th, 2021
42. Completed following NPTEL-SWAYAM Courses
    a. Python for DATA Science in 2021
    b. VLSI Signal processing in 2020
    c. Hardware modelling using Verilog in 2018
    d. VLSI Physical design in 2018
43. Completed following COURSERA courses in the duration of July-Sep 2020.
    a. FPGA Design for Embedded Systems Specialization
    b. Machine Learning Foundations: A Case Study Approach
    c. Python for Everybody Specialization
    d. VLSI CAD Part I: Logic
44. ATAL FDP on "FPGA Based Deep Learning Applications in Signal Processing" from 05th July to 09th July 2021.
45. Virtual Event on "2021 Intelligence in Chip: Tomorrow of Integrated Circuits (ICTIC)", The IEEE CASS Seasonal School, from 1st August to 5th August 2021
46. ATAL FDP on "Research Issues in VLSI Design and Testing" from 02th August to 06th august 2021.
47. ATAL FDP on "Faculty Development Programme on "VLSI -IP DESIGN Approach to SRAM compiler design" from 16th August to 20th august 2021.
48. ATAL FDP on "Nano Electronics and RF Engineering" from 6th September to 10th September 2021.
49. Five-day online workshop on "VLSI Design Using EDA Tools", Organized by department of ECE, Gayatri Vidya Parishad College of Engineering in association with Apply Volt and IETE Visakhapatnam Centre during April 18th -22th, 2022.

5.Academic Contribution and Research & Consultancy:

- 5.1. Invited Lectures: Resource person for RTL Design and Verification webinar Series on 18th, 23rd, 24th and 25th of June 2020.
- Resource person for VLSI Training for II B.tech(2019-2023) ECE

5.2. Articles/Chapterspublished inBooks: Nil
5.3. Bookspublishedassingleauthororaseditor: Nil
5.4. Projects Guided:
    a) UG: 16
    b) PG: 10
5.5. Research Interests: VLSI design, Low Power VLSI, VLSI Testing and Verification
5.6. Ph.D students:
    a) Enrolled:
    b) Submitted:
    c) Awarded:
5.7. Papers published in reviewed Journals:

S.No	Title Of The Paper	Journal Name Vol.No. PP	ISBN/ISSN No	Impact Factor	National/ International

1	Low power design methodology for arithmetic circuits	International journal of engineering sciences & research technology, Volume: 12, issue :4	2277-9655	3.785	International
2	High speed wide fan-in data selector using current comparison domino in synopsys Hspice	International journal of engineering sciences & research technology, Volume: 12, issue:4	2277-9655	3.785	International
3	Implementation of advanced metro ticketing system using i2c driver	International journal of scientific engineering and technology research, Volume:04, issue:37	2319-8885	3.631	International
4	An embedded control system based on rt-linux using priority inheritance mechanism	International journal of electrical electronics and communication, Volume: 18, issue: 4	2048 -1069	0.565	International
5	Low power design using multi bit flip flops	International journal of electrical electronics and communication, Volume: 20 issue: 4	2048 -1069	0.565	International
6	Design and Development of Low Power 90nm Technology Digital Gates using Dual Threshold Transistor Stacking Technique	International Journal of Electrical Electronics and Communication Volume: 20 issue: 4	2048 -1069	0.565	International
7	FPGA implementation of decimal frequency divider using I2C	CiiT International Journal	0974 – 9624		International
8.	ASIC design and Verification of AMBA – APB Protocol using UM	International journal of innovative technology and exploring Engineering Vol:9, Issue:9	2278-3075		Interntaional
9	FPGA implementation of snoopy bus-based cache coherence protocols for dual processor system	International Journal of Modern Education and Computer Science (IJMECS) -Scopus	2075-0161		Interntaional
10	FPGA implementation of secure data transmission for IOT	Design Engineering Year 2021 Issue- 09	0011-9342		Interntaional

5.8. Papers presented at National / International Conferences:

S.No	Title of the Paper	Names of the Conference/ Seminars	National/ International	Period
1	Timing and Synchronization for Explicit FSM based Traffic Light Controller	7th IACC at VNRVJIET, Hyderabad	International	(5-7,Jan 2017
2	FPGA Implementation of FIR Filter Architecture using MCM Technology with Pipelining	2nd International Conference of Emerging Technology (INCET 2021)	International	21s t to 23r d May 2021.

5.9. Sponsored research Projects:Nil

S.No	**Title**	**Agency**	**Period**	**Grant amount**	**Ongoing / Completed**

5.10 Consultancy Projects:Nil

S.No	**Title**	**Agency**	**Period**	**Sanctioned Amount**	**Ongoing / Completed**

6. Awards / Honors received: Selected one of the Best WIT& WIL Scenario of STLD Subject " Metro Rail Scenario" as one of the best Scenarios from the ECE department in 2018.

7. Motto: Every second is a chance to turn our life around