Name : **Dr.P. Kishore**
Designation: Associate Professor
Department: Electronics & Communication Engineering
Mail.I.D : kishore_p@vnrvjiet.in
Experience (in years): Teaching:15 Yrs Research: Others (If any, Specify):

1. Educational / Technical qualifications:

S.No	Level (UG / PG / Ph.D)	Year of passing	Specialization
1	Ph.D	2018	Low Power VLSI
2	PG(M.Tech)	2007	VLSI SYTEM DESIGN
3	UG(B.E)	2004	E.C.E

2. Teaching and Learning:

2.1. Teaching Interests:

Analog Communications, VLSI Design, Low power VLSI, Probability Theory and Random Processes, Signals and Systems, Digital Signal Processing, Digital System Design, Electronic Devices and Circuits, Algorithms for VLSI design automation, Scripting Languages for VLSI design automation.

2.1 Novel Teaching & Learning Techniques adopted: WIT & WIL

2.2 Involvement in curriculum updating / Design:

Updated the contents of CMOS Digital IC design, Prepared the syllabus for CMOS Digital IC design, Low Power VLSI design for P.G.

Prepared the syllabus for Electives under VLSI domain –R18 and R19 batches of U.G

3. Co-curricular and Extra-Curricular Activities

3.1. Interests and Hobbies: Internet browsing and Playing Cricket

3.2. CCA/ECA Organized: Coordinator for organizing badminton in sports fest 2015.

3.3. CCA/ECA participated: Nil

3.4. Counseling and Mentoring Activity:

Counseling being done for the allotted students and helping in their personal and academic problems.

3.5. Committees involved in:

Department level:

- Coordinator PG VLSI since March 2021.
- Member of Department Research Committee since November, 2019
- Member of Anti Ragging & Disciplinary Committee 2018-19 academic year.
- Member of Board of Studiessince 2018-19 academic year.
- Member of Academic Development Committee since March 2018.
- Department NBA coordinator (2017-21)
- Coordinator CRC for Ist and 3rd Years(2017-21)
- Member of Project review committee for IV-ECE-2.(2016-21)
- Member of Project Review Committee (PG-VLSI System Design).
- Member of Program Assessment Committee (PG-VLSI System Design).
- Member of Program Assessment Committee (UG-ECE).
- Member of Research Project Proposal Reviews
- Coordinator for Invigilation duties since 2014 to till date.
- Member of Website and Communication Committee of IACC-2017.
- Coordinator of TEQIP-II.(2014-15)
- Coordinating Member of P.G school (VLSI) during 2015-16.
- Coordinator of UG NBA application work during 2014-16.

Institute Level:

- Faculty Advisor for IEEE Circuits and Systems society of VNR IEEE Student branch.
- Convener of Open House project Expo-2019 and 2020.
- Faculty Advisor for IEEE Circuits and Systems society of VNR IEEE Student branch.
- Coordinator of CONVERGENCE-2K18
- Convener of CONVERGENCE – 2K18(Reloaded), October 2018
- Liaison officer for NAAC-cycle II peer team visit-July 2018.
- Member of NAAC –A++ Committee.
- Member of Research and Development Committee since March 2018
- Member of Refreshments committee for Sports fest -2018
- Member of Anti Ragging &Disciplinary Committee since 2017-18
- Coordinator of CONVERGENCE-2K17
- Member of Refreshments committee for Sports fest 2016, 2017, 2018, 2019, 2020, 2022.
- Member of disciplinary committee for Syntilatunz and Annual day celebrations-2016

4. Conference / Workshop / Seminar / Guest Lectures:

4.1. Conducted:

- Organized a Distinguished lecture on "State of the art Silicon VLSI: Industrial face of Nanotechnology" by Dr. Michael Shur on 01-06-2021 in association with IEEE Hyderabad section.
- Organized a webinar on "Demystifdying Electromagnetics" in association with IEEE VNRVJIET SB and CASS SBC on 03-05-2021.
- 2-week FDP on " System Design Methodologies for Embedded, IoT, AI, & HPC using Intel FPGA (Industry supported- Intel India)" jointly organized by E&ICT Academy, NIT Patna in during 19th April 2020 to 30th April 2020, in association with NIT Patna, MNIT Jaipur and IIT Guiwahati.
- Organized a webinar on "IoT is the new IT" in association with IEEE VNRVJIET SB and CASS SBC on 05-10-2020.
- A 10 Day FDP on "Digital tools for writing, authoring and reviewing manuscripts" during 21st September 2020 to 2nd October 2020, in association with NIT Patna and MNIT Jaipur.
- Organized a two week FDP on " Python Programming-An Industrial Perspective" in association with NIT Patna from December 2 – 6, 2019 through National Knowledge Network under the "Scheme of financial assistance for setting up of Electronics and ICT Academies" by the Ministry of Electronics and InformationTechnology (MeitY), Government of India. This programme is endorsed by AICTE /UGC / NBA.
- Organized a two day workshop on "IoT and Drones", during 26th -27th January 2019 in association withleadingindia.ai, in the department of ECE, VNR VJIET in association with Leadingindia.ai of Bennett University.
- Organized a two day workshop on "Machine Learning" during 5th -6th October 2018, in the department of ECE, VNR VJIET, and Hyderabad.

- Organized one day workshop on "XILINX FPGAs" during 17th October 2014, in the Department of ECE, VNR VJIET, and Hyderabad.
- Organized a workshop on "PCB Design & Fabrication" under industry oriented skill up graduation program during 11th -19th January 2016,in the Department of ECE,VNR VJIET, Hyderabad

4.2 Attended:

- Two week online FDP on "System Design Methodologies for Embedded, IoT, AI, & HPC using Intel FPGA" jointly organised by Electronics and ICT Academies held from 19th April to 30 April, 2021 under the "Scheme of financial assistance for setting up of Electronics and ICT Academies" of the Ministry of Electronics and Information Technology (MeitY), Government of India.
- 5 Day PDP on " Basics of Python Programming" Organized by VNRVJIET during 9th-13th November 2020.
- Successfully completed the AICTE Sponsored One Week Online Short Term Training Program on ICT Tools for Engineering College Teaching and Outcome Based Learning Organised by Department of Electronics & Communication Engineering, Raghu Institute of Technology (Autonomous) During 5th October - 10th October,2020.
- Two week online FDP on "Demystifying 5G RF ASICs" jointly organised by Electronics and ICT Academies held from 24 August to 04 September, 2020 under the "Scheme of financial assistance for setting up of Electronics and ICT Academies" of the Ministry of Electronics and Information Technology (MeitY), Government of India.
- Two week online FDP on "Python Programming" jointly organised by Electronics and ICT Academies held from 7th September, 2020 to 18th September 2020 under the "Scheme of financial assistance for setting up of Electronics and ICT Academies" of the Ministry of Electronics and Information Technology (MeitY), Government of India.
- participated & completed successfully AICTE Training And Learning (ATAL) Academy Online FDP on " Control Systems & Sensors Technology" from 17-08-2020 to 21-08-2020 at Government College of Engineering, Srirangam.
- Attended a 5 Day PDP on "NBA in a Nutshell" organized by IEEE VNRVJIET SB during 27th July 2020 to 31st July 2020.
- One week FDP on "Artificial Intelligence and Machine Learning"Organized by VNRVJIET during 13th-17th July 2020.
- One Week FDP on "VNR Initiatives and awareness on OBE"Organized by VNRVJIET during 6th-11th July 2020.
- One Week FDP on "Effective Onlione Teaching using ICT tools"Organized by VNRVJIET during 29th June-04th July 2020.
- Participated & completed successfully AICTE Training And Learning (ATAL) Academy Online FDP on "Artificial Intelligence" from 27-04-2020 to 01-05-2020 at Motilal Nehrunational Institute of Technology Allahabad.
- AICTE Sponsored Five day Faculty Development Programme on"Research Methodology and IPR", during 5th August 2019 to 9th August 2019 Organized by JNTUH Hyderabad.
- One week workshop on "Wireless and Mobile Communication" during 1st -6th July 2019,Jointly Organized by Electronics and ICT Academy & NIT Warangal in association with department of ECE, VNR VJIET, Hyderabad.
- Five day workshop on "VLSI Chip Design Hands on using Open Source EDA"during 8h -12th July 2019 funded by MeitY, Govt.of India organized by Electronics and ICT Academy, NIT Patna in association with department of ECE, VNR VJIET, Hyderabad.

- Five day workshop on “Robotics &AI”during 24th -28th June 2019 funded by MeitY, Govt.of India organized by Electronics and ICT Academy, NIT Patna in association with department of ECE, VNR VJIET, Hyderabad.
- Five day workshop on “Embedded Systems & Interfacing(Hands-On)”, during 10h - 14th June 2019 funded by MeitY, Govt.of India organized by Electronics and ICT Academy, NIT Patna in association with department of ECE, VNR VJIET, Hyderabad.
- Two day workshop on “IoT and Drones”, during 26th -27th January 2019 in association withleadingindia.ai, in the department of ECE, VNR VJIET in association with Leadingindia.ai of Bennett University.
- Attended a workshop on “Artificial Intelligence and Deep Learning” organized by SR Engg College,Warangal, during 17th June 2018 to 19thJune 2018.
- Attended a Two week ISTE STTP on “CMOS Mixed Signal and RF VLSI Design” organized by IITKharagpur at VNRVJIET, Hyderabad,30th January 2017 to 04th February 2017.
- Attended a one week national workshop on “Recent Advancements in VLSI Technology and Design Using EDA Tools(VLSITP2016)”organized by JNTUK, Kakinada during 20 th - 24 th July 2016.
- Participated inTEQIP-II sponsored 3 day Faculty development programme on "VLSI Digital signal processing" Organized by GRIET during 28/01/2016 to 30/11/2016.
- Attended a faculty development programme on "VLSI SYSTEM Design " Organized by MLRITM, Hyderabad on 28/11/2015.
- Attended a TEQIP-II sponsored training programme on "VLSI Design flow using CAD tools" Organized by VNRVJIET during 27/07/2015 to 07/08/2015.
- Attended a Workshop on "Control Systems" under the National Mission on Education through ICT (MHRD, Govt. of India) from during 02/12/2014 to 12/12/2014 in the GRIET, Hyderabad.
- Attended a Workshop on "Wireless sensor nodes" organized by Dept .of ECE,VNRVJIET, Hyderabad in collaboration with ITRA,New Delhi during 19th to 20th December 2014.
- Attended a Workshop on "ASIC Design Flow Using Industry Standard EDA Tools"organized by Dept. of ECE, VNRVJIET, Hyderabad during 21st To 27th Aug 2014.
- Attended a workshop on “VLSI Design” sponsored by AICTE and organized by Department of Electronics and communication Engineering,VNRVJIET,Hyderabad during 20th May 2013 to 01st June 2013.
- Attended a workshop on “MATLAB & its applications in Communications and Signal Processing” organized by Department of Electronics and communication Engineering , Andhra University College of Engineering(A), Visakhapatnam in association with the Academy of Design and Architecture, Hyderabad during 12th to 13th Nov, 2011.
- Attended a two week faculty updation program on “System Design using FPGA”(FUTURE) sponsored by MHRD organized by CDAC,Hyderabad during 17th May to 29th May 2009.
- Participated in a one week short term course on “Technology CAD for VLSI Design”sponsored by AICTE and MHRD organized by Department of E&EC,IIT Kharagpur and Department of ECE,AUCE(A) during 1st June to 7th June 2009.
- Participated in a workshop on “Advances in Signal & image processing” organized by Dept. of ECE,.JNTU college of engineering , Kakinada during 20th -21st October 2008.

- Participated in a workshop on "Electromagnetics and Applications" organized by Dept. of ECE&EEE .BVC engineering college, Odalarevu during 8th -9th March 2008.
- Participated in a "workshop on Electromagnetics" organized by Dept. of ECE,.ANITS, Visakhapatnam during 20th -21st October 2007.

5. Academic Contribution and Research & Consultancy:

5.1. Invited Lectures: Delivered a Lecture in a 5 Day PDP on "NBA in a Nutshell" organized by IEEE VNRJIET SB during 27th July 2020 to 31st July 2020.

5.2. Articles/Chapterspublished inBooks: NIL

5.3. Bookspublishedassingleauthororaseditor: Design of Low Power and High Performance Logic Circuits, Lambert Academic Publisher,2018. © Kishore Pinninti, ISBN:978-613-9-44568-4

5.4. Projects Guided:

a) UG: 20

b) PG: 03

5.5. Research Interests:

Low power VLSI , VLSI architectures for Video Processing, Fault Tolerance.

5.6. Ph.D students:

a) Enrolled: NIL

b) Submitted: NIL

c) Awarded: NIL

5.7. Papers published in reviewed Journals:

S.No	Title of the Paper	Journal Name Vol.No. PP	ISBN/ISSN No.	Impact Factor/ Citation Index	National/ International
1	Implementation of Multi Bit Even Parity Generator and Checker Circuits Using Quantum Cell Automata (QCA) Based Majority Gates	Design Engineering,Issue:09, pp. 6740-6751	ISSN:0011-9342	1.409	International
2	Low Area and Reduced Delay of Encoded Data Using Modified BWAR	International Journal of Advanced Science and Technology. pp. 6181-6188	ISSN: 2005-4238	0.475	International
3	Performance analysis of OFDM and FBMC over selective channels,	Materials Today: Proceedings, pp. 4237–4242.	ISSN:2214-7853	H-index-27	International
4	Detection and analysis of Alzheimer's disease using various machine	Materials Today: Proceedings	ISSN:2214-7853	H-index-27	International

	learning algorithms				
5	Design of automated identification of alcoholic drivers in intoxicated state	Materials Today: Proceedings	ISSN:2214-7853	H-index-27	International
6	Design of high performance adder using modified GDI based full adder	Journal Of Mechanics Of Continua And Mathematical Sciences	ISSN:0973-8975	2.8	International
7	Low Area and Reduced Delay of Encoded Data Using Modified BWAR,	International Journal of Advanced Science and Technology, pp. 6181-6188	ISSN: 2005-4238	SJR:0.18 Impact factor : 0.41	International
8	Design of Low Power and High Performance Phase Detector Using MOD- GDI Technique.	International Journal of Research, pp.60-65	ISSN NO: 2236-6124	5.7	International
9	FPGA implementation of Fault Diagnosing of Interconnects in SRAM Based FPGA's,	Journal of Applied Science And Computations, pp.199-203	ISSN NO: 1076-5131	5.8	International
10	Design of Low Power and High performance NAND Based Flip-Flops Using Mod- GDI Technique&	Journal of Applied Science And Computations, pp.2027-2031	ISSN NO: 1076-5131	5.8	International
11	FPGA Implementation of VLSI Architecture for Random Early Detection Gateways for	International Journal of Research, pp. 2309-2315	ISSN NO: 2236-6124	5.7	International

	Congestion Avoidance				
12	An Efficient Test Data Compression Scheme Using Optimal Selective Huffman Coding	International Journal of Research, pp.2107-2112	ISSN NO: 2236-6124	5.7	International
13	Alzhemer's disease detection using different machine learning algorithms	The International journal of analytical and experimental modal analysis	ISSN NO:0886-9367	6.3	International
14	Benign and Malignant Tumor Classification using Machine Learning Technique	International Journal of Recent Technology and Engineering (IJRTE)	ISSN: 2277-3878	6.04	International
15	Implementation of Symbol Synchronizer Using ZynqSoc	International Journal of Management, Technology and Engineering, pp. 476-487.	ISSN NO : 2249-7455	6.3	International
16	Design of Low Power and High Speed Braun Multiplier using Modified Gate Diffusion Input Technique	International Journal of Computer Science and Information Security (IJCSIS), Vol. 14, No. 11, pp.408-412.	ISSN 1947-5500	0.519	International
17	Low power and high speed carry save adder using modified gate diffusion input technique	ARPN Journal of Engineering and Applied Sciences, VOL. 11, NO. 21,pp. 12653-12659.	SSN 1819-6608	SJR:0.2	International
18	Design of Low voltage, Low Power and High Speed Logic Gates Using Modified GDI Technique	International Journal of Latest Trends in Engineering and Technology (IJLTET), Vol 7 Issue 2, pp.435-444.	ISSN: 2278-621X	0.68	International
19	A Novel Low power and Area Efficient Carry-Lookahead Adder	International Journal of Science and Research	ISSN 2319-7064	4.438	International

	Using MOD-GDI Technique	(IJSR);Vol.4,Issue-5,pp1205-1210.			
20	Motion Estimation in Mpeg-4 Video Sequence Using Block Matching Algorithm	International Journal of Engineering Science and Technology (IJEST); Vol.3,Issue 12,pp. 8466 - 8472.	ISSN: 0975-5462.	3.14	International
21	Implementation of Dual-Core Multithreaded Processor on Xilinx Spartan-III FPGA	International Journal of Engineering Science and Technology (IJEST), Vol.3,Issue 12, pp.8473 - 8478.	ISSN: 0975-5462.	3.14	International
22	Image Segmentation of Moving Image Sequence Using Motion Vector Estimation Algorithm	International Journal of Electronics and Communication Technology Science and Technology (IJECT); Vol. 3, Issue 2,, pp. 248-254	ISSN : 2230-7109,	.0413	International

5.8. Papers presented at National / International conferences:

S.No	Title of the Paper	Names of the Conference/ Seminars	National/ International	Period
1	Mental Health Disorder Analysis Using Convolution Neural Network Based Speech Signal Model With Integration Of Artificial Intelligence	4th International Conference on Recent Developments in Control, Automation & Power Engineering (RDCAPE)	International	7th -8th October 2021
2	Satellite based Road Tagger GPS Radio-Navigation system with Integration of Artificial Intelligence	4th International Conference on Recent Developments in Control, Automation & Power Engineering (RDCAPE)	International	7th -8th October 2021
3	"Implementation of digital phase locked loop using CMOS technology"	First International Conference on Advances in Electrical, Computing, Communications and Sustainable Technologies (ICAECT 2021)	International	19th -20th February 2021

4	A Modified Novel Signal Flow Graph and Memory-Based Radix-8 FFT Processor Design	the Fourth International Conference on Smart Computing and Informatics Smart Computing Techniques and Applications		5^{th} to 6^{th} June 2020
5	A Review on Comparative Analysis of Add-Shift Multiplier and Array Multiplier Performance Parameters	Proceedings of International Conference on Advances in Computer Engineering and Communication Systems	International	13^{th} -14^{th} Auguts 2020
6	Performance Comparison for Ripple carry adder using Various Logic Design	International Conference on Advances in Signal processing, Power, Embedded, Soft Computing, Communication and Control Systems (ICSPECS-19)	International	11th-12th January 2019.
7	Riverbed Modeler Simulation based performance analysis of routing protocols in mobile	International Conference on Advances in Signal processing, Power, Embedded, Soft Computing, Communication and Control Systems (ICSPECS-19)	International	11th-12th January 2019.
8	Low power and High speed synchronous carry generate adder	International Conference on Advances in Signal processing, Power, Embedded, Soft Computing, Communication and Control Systems (ICSPECS-19)	International	11th-12th January 2019.
9	Low Power and High Speed Optimized 4-bit Array Multiplier using MOD-GDI Technique	7th IEEE International Advance Computing Conference (IAC C-2017)	International	5th-7th January 2017
10	Design and Implementation of Remote Terminal for MIL-STD-1553 B	7th IEEE International Advance Computing Conference (IAC C-2017)	International	5th -7th January 2017
11	Design of Low Power and Propagation Delay NAND Based Flip-	7th IEEE International Advance Computing Conference (IAC C-2017)	International	5th -7th January 2017

	Flop Using Mod-GDI Technique			
12	Design and Implementation of Low Power MIL STD 1553B Bus Controller	International Conference on Micro-Electronics, Electromagnetics and Telecommunications (ICMEET-2016)	International	6th - 7thJanuary 2017
13	Low power and optimized Ripple carry adder and carry select adder using MOD-GDI Technique	International Conference on Micro-Electronics, Electromagnetics and Telecommunications (ICMEET-2015)	International	18th - 19th December 2015
14	MPEG-4 Motion Estimation Using Block Matching Algorithm	International Conference on Aerospace Electronics, Communications & Instrumentation (ASECI-2010).	International	6th - 7thJanuary,2010
15	Fault analysis in FPGA Using Phase Path Method	International Conference on RF and Signal Processing systems (RSPS-2010)	International	7th to 9th January 2010
16	Design of High Speed Routers using RED Algorithm	Proceedings of the 2011 International Conference on Communication, Computing & Security,2011, pp- 106-109, ACM ISBN: 978-1-4503-0464-1.	International	12th -14th February 2011
17	VLSI Architecture for the efficient estimation of moving Components in a Video Image Sequence	International Conference on Electronic Systems (ICES-2011)	International	07th -09th January 2011
18	Implementation of Dual-Core Power 5 Fine Grained Multithreaded Processor on Spartan-III FPGA	IEEE Conference proceedings of International Conference on Devices and Communication	International	24th -25th February 2011
19	Image Segmentation of a Moving Image Sequence using Motion Vector Estimation Algorithm	National Conference on Advances in Communication, Navigation and Computer Networks (ACNCN-2012)	National	17th to 18thMarch 2012.
20	VLSI Architecture for random early Detection	National Conference on recent advances in DSP, Embedded Systems, VLSI, Image	National	Nov 13th - 14th ,2010

	Gateways for Congestion Avoidance.	Processing, Communications and Electronics Engineering (DEVICE-2010)		
21	VLSI Architecture for Data Management in DSP Processor	National Conference on Communication Technologies (NCACT-2010)	National	3rd -4th December 2010
22	FPGA Implementation of High Speed Crypto-System Using AES Algorithm	National Conference on Automation, Communication & Computing (NCACC-2010)	National	9th -10th December 2010
23	Image Segmentation of a moving Image Using Motion Vector Estimation Algorithm	National Conference on Advances in Signal Processing(NCASP-09)	National	November 20th -21st ,2009.

5.9. Sponsored research Projects:

S.No	Title	Agency	Period	Grant amount	Ongoing / Completed
1	Development of Low power and High speed FPGA based IP Core mini ace architecture compatible to Data device corporation .	AICTE	3 YEARS	14.35294 Lakhs.	Ongoing

5.10 Consultancy Projects:

S.No	Title	Agency	Period	Sanctioned Amount	Ongoing / Completed
1	IP Core Development Of MIL STD 1553 for RT and MT Terminals"	Ananth Technologies Ltd	1 YEAR	4.24 Lakhs.	Completed

6. Awards / Honors received:

- Dr. Sarvepalli Radha **Krishna Distinguished Scientist Award-2021**in appreciation of the dedication and commitment in Technology and Research in ECE conferred on 5th September 2021 by Center for Professional Advancement Continuous Education(CPACE).
- Executive Committee Member of Circuits and Systems Society, IEEE Hyderabad Section for 2020-21& 2021-22.
- Received Best Teacher award at ANITS for the academic year 2010-11.
- Elevated to IEEE Senior member in April 2020.

7. Motto: Success is not final, failure is not fatal: it is the courage to continue that count.