FACULTY DEVELOPMENT PROGRAMME (FDP)

8th -12th July, 2019

On

VLSI Chip Design Hands on using open source EDA

Jointly Organized by

ELECTRONICS & ICT ACADEMY, NATIONAL INSTITUTE OF TECHNOLOGY PATNA – 800005

&

Department of Electronics and Communication Engineering

VNR Vignana Jyothi Institute of Engineering & Technology, Hyderabad

(Sponsored by MeitY, HRD division, Ministry of ICT, Govt. of India)

Preamble:

Ministry of Electronics and Information Technology (MeitY), Govt. of India in November, 2014 has approved a "Scheme of Financial Assistance for setting up of Electronics and ICT Academies" over a period of 5 years for faculty/mentor development and enhanced the employability of the students in various streams. As per the scheme approval Seven (07) Electronics and ICT Academies have been set up and NIT Patna is one of them.

Objective of the Academy –

- To focus on improving the quality of faculty of institutes, colleges in the respective states by organizing FDP for –

· Engineering, Polytechniques etc in emerging areas of Electronics and IT.

MeitY and all E & ICT Academies have planned again for the **Summer Course-2019 through NKN** under E & ICT Academies **from 20th May to 12th July, 2019.**

About Summer Courses:

Faculty Development Programmes in core areas of Electronics and Information & Communication Technology (ICT) streams have been planned by academies for delivery during Summers (i.e., May – July 2019). All these summer courses will be offered through National Knowledge Network (NKN) based Video Conferencing, with lectures delivered by invited experts from IITs, NITs, IIITs and other premier institutes/industries. In addition, local course coordinators at respective academies /identified remote centres will take care of sessions on design orientation/activity linked problems/ assignments/ case studies and quiz test(s). All seven EICT Academies will host the participants simultaneously along with some select remote centres all over our country, through NKN-VC infrastructure. Candidates could attend the training programme at Academy locations or at identified remote centres as per the convenience.

Course Objectives:

This course is designed to provide an exposure to the fundamentals of VLSI chip designing. Participants will learn Floor Planning, placement and global routing. Hands-on training and practice sessions will help participants gain confidence on Analog and Mixed Signal Circuits, their simulation and implementation including sessions on chip designing using EDA Tools. The course will be useful for faculty of engineering and sciences who are interested in the learning VLSI chip designing.

Major Course Contents:

- **VLSI design, SoC Design**
- **Floor planning & timing analysis**
- **Placement, Clock tree synthesis**
- **Global routing, Detailed routing**
- **Analog and Mixed Signal Circuits: Specifications, Design, Layout & GDS**

Resource Persons:

- **Dr. Imon Mondal, IITK**
- **Prof. Sachin Patkar, IITB**
- **Dr. Anand Bulusu, IITR**
- **Dr. H. S. Jatana, SCL**
- **Dr. Subhakumar Reddy A., VEDA-IIT**

Eligibility:

The programme is open to the teachers of engineering colleges from Electronics and communication Engineering. Research scholars and Industry personnel working in the concerned/allied discipline can also attend.

Registration Fee for each Summer Course:

No Registration fee is charged for attending this programme planned at any designated academies/Remote centres. However, candidate should submit a **Demand Draft of Rs.1000/- in favor of "Director, NIT Patna" payable at Patna** along with application form and the same will be handed over to the participant on the last day of the training. Certificate for participation as well as for Satisfactory performance will be given to the participants subject to fulfillment of attending all sessions, submission of assignments and clearing the test(s).

Accommodation:

No TA/DA will be paid to the participants. Working Lunch, Tea & Snacks would be provided during the training at VNRVJIET campus.

Selection Criterion:

Selection will be done based on ***first-cum-first-serve basis*** and the confirmed candidates will be notified immediately. The maximum number of participants will be **40 (forty**). Additionally 10 participants from industry are allowed to participate.

Candidates will be issued certificates on successful completion of the course. Reservations of seats are followed for selecting candidates as per GOI norms.

Venue: VNR Vignana Jyothi Institute of Engineering &Technology, Hyderabad.

Important dates:

Spot registrations also will be accepted based on the number of registrations

About NITP & VNR VJIET

National Institute of Technology Patna is the 18th National Institute of Technology created by the Ministry of H.R.D. Government of India after rechristening the erstwhile Bihar College of Engineering Patna on 28. 01. 2004. NIT Patna marked its humble beginning in 1886 with the establishment of pleaders survey training school which was subsequently promoted of Bihar College of Engineering Patna in 1924. This made this institute the 6th Oldest Engineering Institute of India Institution imparting technical education of a very high standard leading to the B.Tech degrees in various branches of engineering and M.Tech. and Ph.D. programmes in various specializations.

"Valluripalli Nageswara Rao (VNR) Vignana Jyothi Institute of Engineering and Technology"(**VNRVJIET**) was established by "VIGNANA JYOTHI. "Vignana Jyothi"was carved and created in the year 1991 by a dedicated group of Industrialists, Entrepreneurs and Professionals who felt that education is the light that wipes out the darkness of an uncertain future among the youth and were determined to impart quality education to them without profit motive. An Autonomous Institute, approved by AICTE, affiliated to JNTUH was established in the year 1995 and is accredited by NAAC with A^{++} - Grade and also 7 UG & 4PG programmes are accredited by NBA. UGC recognized VNR VJIET as College with Potential for Excellence Status. Being one of the most preferred colleges in T.S., VNRVJIET is well known for its discipline, technical excellence, infrastructure, record student performance, research activities, etc.

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APPLICATION FORM

Paste Passport Photograph here)

1. Name:

   Gender: M/F

2. Designation:

3. Institution:

4. Email:

6. Address for Correspondence:

7. Mobile No:

8. Educational Qualifications with specialization:

9. Subjects taught so far:

10. No. of refresher courses/workshops attended:

11. Experience (in years)
    Teaching:
    Research:
    Industry:

12. Accommodation required: YES / NO

13. Do you belong to SC/ST: YES/NO

Declaration
The information provided is true to the best of my knowledge. I agree to abide by the rules and regulations of the FDP and shall attend the course for the entire duration. I also undertake the responsibility to inform the Coordinator in case, I am unable to attend the course.
Place:
Date: Signature of the applicant

Coordinators

Dr.Bharat Gupta
Assistant Professor, Dept. of ECE
Electronics & ICT Academy,
National Institute of Technology Patna

Dr.S. Rajendra Prasad
Professor Dept. of ECE, VNRVJIET

Dr. Pushpa Giri
Asst. Prof. Department of ECE, VNRVJIET

For more information visit:
http://www.nitp.ac.in/uploads/FDP_NKN_Summer_2019_Brochure.pdf

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